# 爲希科技
# Sparatn3E
# XC3S250E-PQ208
# 3S250E 實驗板
# 使用手冊

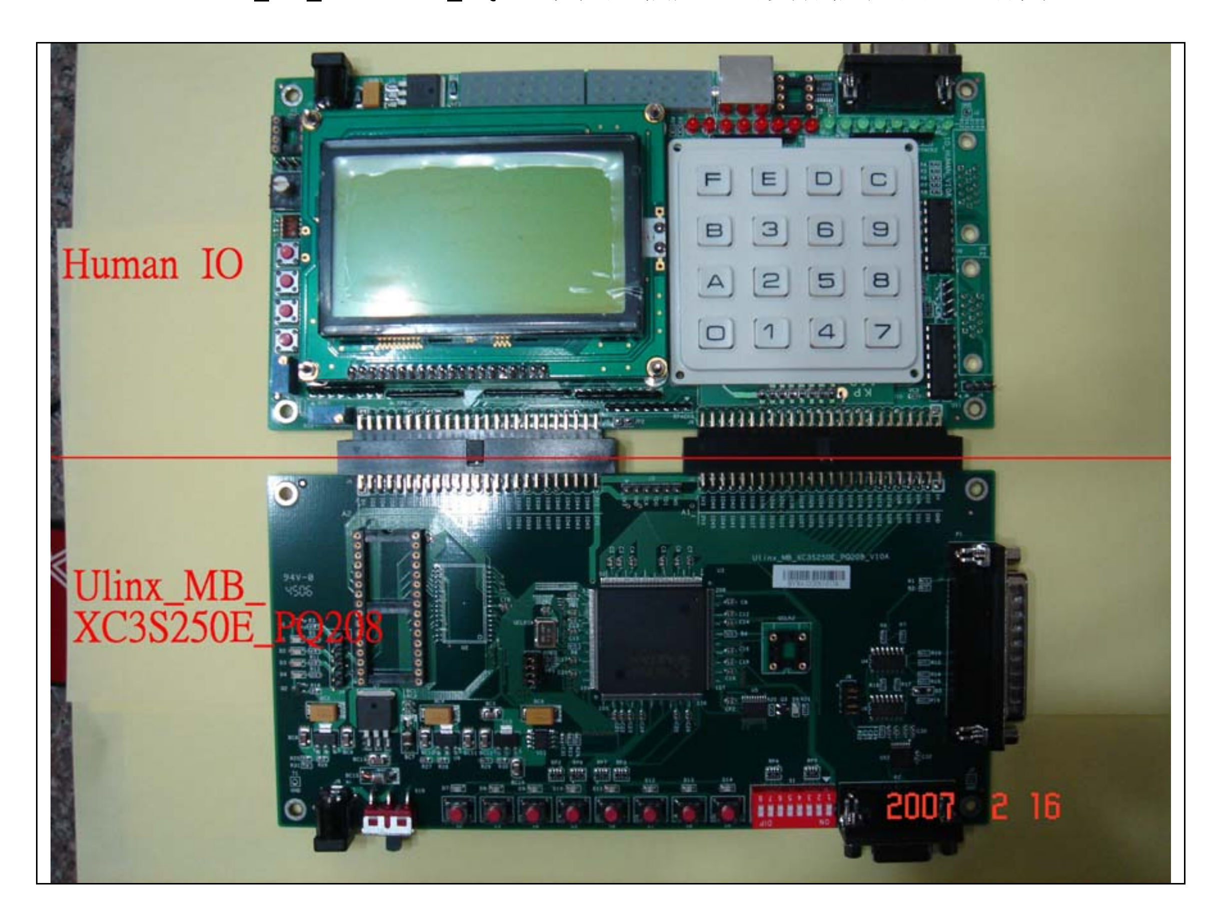
2007.Jan.15 .V1.0

**Ulinx Corp.**

爲希科技有限公司的UBD-Spartan3E-ST3E實驗板提供FPGA使用者一個完整且容易上手的實驗平台.這份手冊將會含括這片實驗板上所有元件的設定及特性說明.

## 主要元件及功能

Ulin_MB_XC3S250E 實驗板由兩塊板子組合而成,上板爲 HUMAN_IO,下板爲 Ulinx_MB_XC3S250E_PQ208,組成一個完整的實驗板,如圖 1-1 所示.



# 第一章 : Ulinx_MB_XC3S250E_PQ208 規格

Ulinx_MB_XC3S250E_PQ208 FPGA 板包含了以下主要元件:

● 25 萬邏輯閘的 Xilinx Spartan-3E XC3S250E FPGA 包裝爲 PQFP 208 隻腳位 (XC3S250E-4-PQ208)
. 內含 12 個 18K-bit 的 Block RAMs (共 216K bits)
. 內含 12 個 18x18 硬體乘法器
. 內含 4 個 Digital Clock Managers (DCMs)
. 內含 158 個 可用腳位
● RS-232 界面
● PROM XCF02S-VO20
● 40MHz 的振盪晶體.
● 一個使用者振盪晶體的 Socket
● 92 點 User IO,可連接 Human IO,或連接使用者設計的板子.
● 8 個 DIP switch
● 8 個 LED 輸出界面
● 8 個 按鍵輸入
● 單一電源輸入( +5V/ 3A )
.提供板子上三組電源使用 ( 1.2 V , 2.5 V , 3.3 V 與一預留的 1.8V)
● JTAG 界面
提供多種燒錄程式的界面

Human_IO 板包含了以下主要元件:

● LCD 液晶螢幕(128 x 64 Pixels)
(可以選購 16 x 2 Text Mode 液晶螢幕)
● 16 字按鍵(4 x 4 矩陣形,可以輸入 0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F 等字元).
● 16 個 LED 輸出介面(8 個綠色 LED,8 個紅色 LED)
● 4 個 按鍵輸入.
● 4 個 DIP Switch 輸入
● 8 個七節燈管顯示輸出.
● VGA 輸出介面.
● PS2 輸入介面.
● Rotary Switch 輸入.(可以設定 0,1,2,3,4,5,6,7,8,9)
● 4 個頻道 DAC 輸出(LTC2624)
● 2 個頻道 ADC 輸入(ADC0832)
● IIC 介面(24C02).

# 產品外觀



# 第二章 ：Ulinx_MB_XC3S250E_PQ208

Ulinx_MB_XC3S250E_PQ208 爲 MB_XC3S250E 的主板,包含電源,FPGA,LED…等週邊介面,再利用 J1,J2 連接 Human_IO 板,本章節主要是敘述 MB_XC3S250E 主板相關週邊電路的相關說明.

## 2-1. 電源.

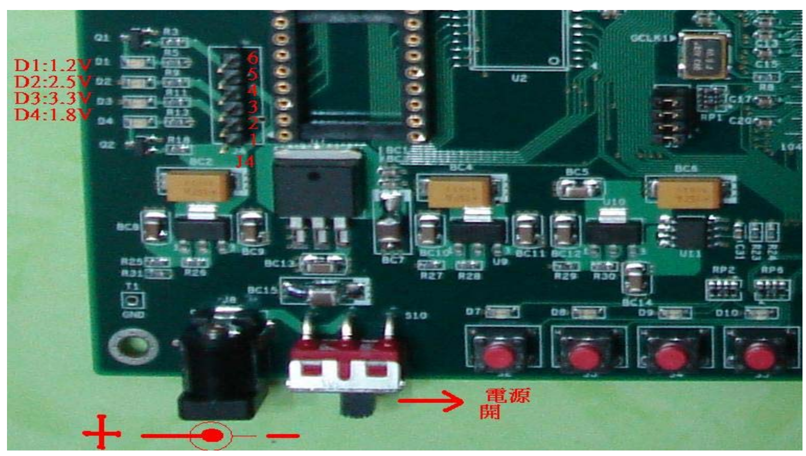
電源插頭 J8 爲外部 5 V 輸入,內正外負的接頭,提供板子的電源輸入,在 J8 的右邊爲:S10 的切換開關, S10 切到右邊時,電源開啓;S10 切到左邊時,電源關閉.

Ulinx_MB_XC3S250E 以內部的穩壓器,將+5V 穩壓成+3.3V,+2.5V,+1.8V,+1.2V 等四種電源,其中+1.8V 爲預留未來使用,而+3.3V,+2.5V,+1.2V 則提供 Ulinx_MB_XC3S250E 板子使用,這四種電源則有 D1,D2,D3,D4 綠色 LED 顯示電源正常.

| |
|---|
| D1:板子上 1.2V 的電壓正常時時 ；D1 綠色 LED 爲亮<br>D2:板子上 2.5V 的電壓正常時時 ；D2 綠色 LED 爲亮<br>D3:板子上 3.3V 的電壓正常時時 ；D3 綠色 LED 爲亮<br>D4:板子上 1.8V 的電壓正常時時 ；D4 綠色 LED 爲亮 |

另外這四種電源,加上+5V 電源,則可以由 J4 輸出.

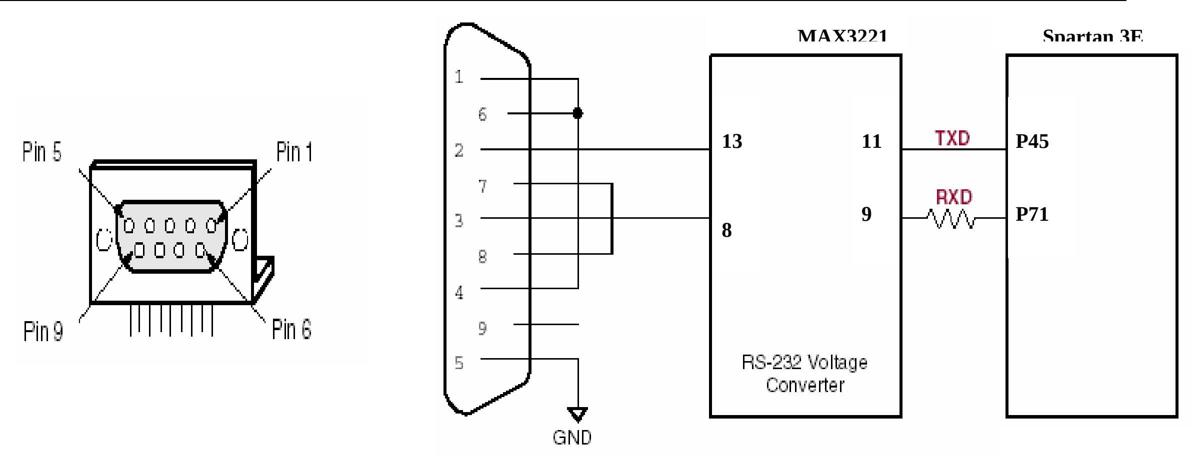
| J4 Connector | Pin | Pin Name | Signal | Comment |
|---|---|---|---|---|
| | 6 | Ground | 電源的地電位 | |
| | 5 | 1.2V | 1.2V 電源 | |
| | 4 | 1.8V | 1.8V 電源 | |
| | 3 | 2.5V | 2.5V 電源 | |
| | 2 | 3.3V | 3.3V 電源 | |
| | 1 | 5V | 5V 電源 | |

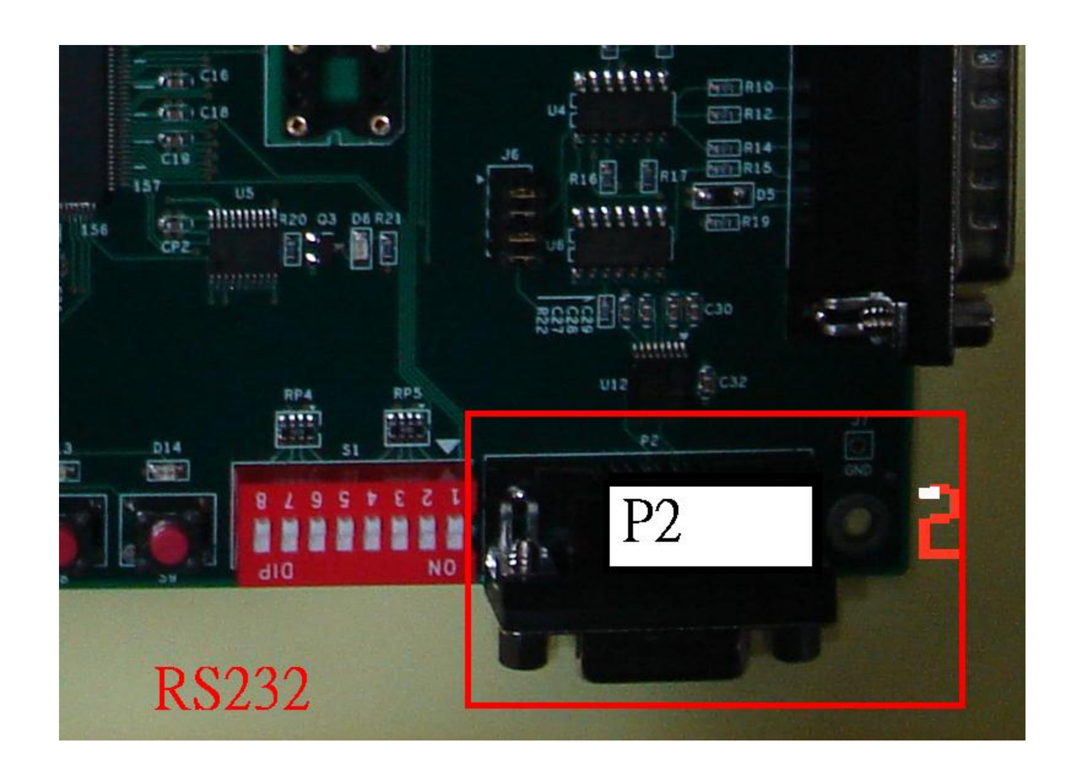



## 2-2. RS232 介面

RS232 介面提供 Ulinx_MB_XC3S250E 板子與 PC 個人電腦之間串列傳輸的介面,板子上的 P2 就是 RS232 接頭,爲一個 DB9 母接頭,只要以 1 對 1 的連接線連接 P2 與 PC 個人電腦串列介面.

```
NET    "RS232_TX"    LOC = "P45"    ;
NET    "RS232_RX"    LOC = "P71"    ;
```

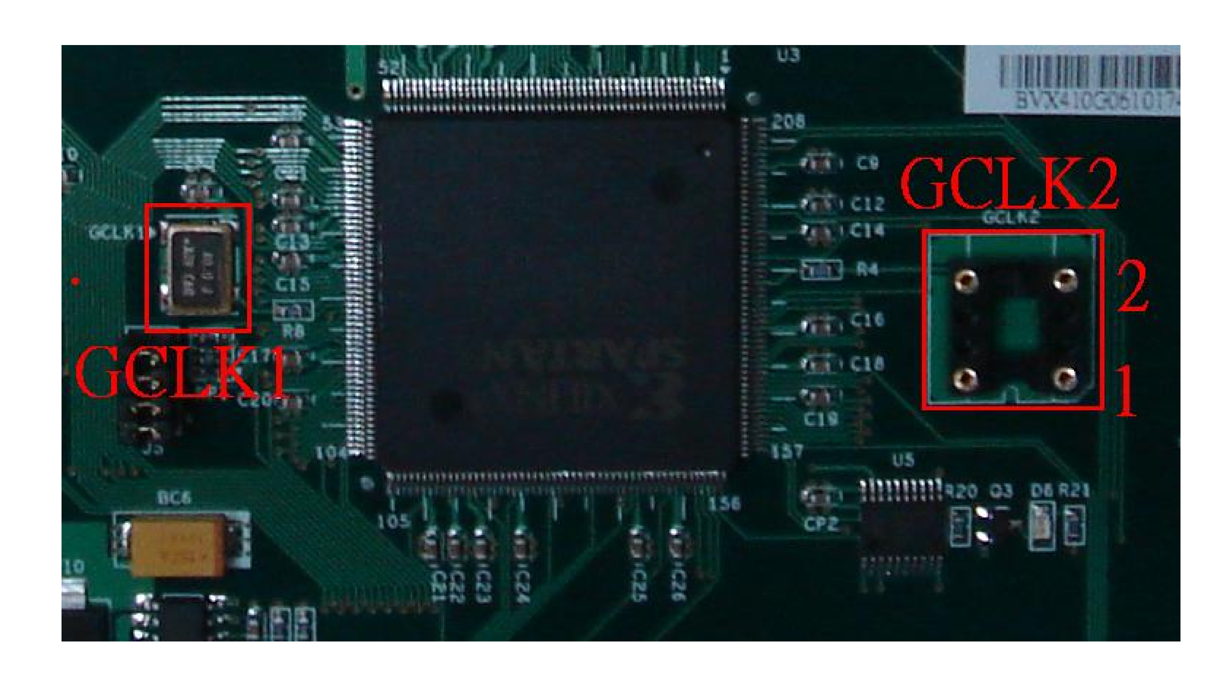





## 2-3. CLOCK 時脈週期

實驗板上有兩個 CLOCK 輸入,板子上的 GCLK1 為 40MHz 的振盪晶體,接到 FPGA 的 Pin-80,而 GCLK2 則提供使用者自行提供使用者所需的振盪晶體,此接腳接到 FPGA 的 Pin-183.

```
NET    "GCLK1"    LOC = "P80"    ;
NET    "GCLK2"    LOC = "P183"    ;
```




## 2-4. PUSH_BUTTON 與 DIP_SWITCH 輸入

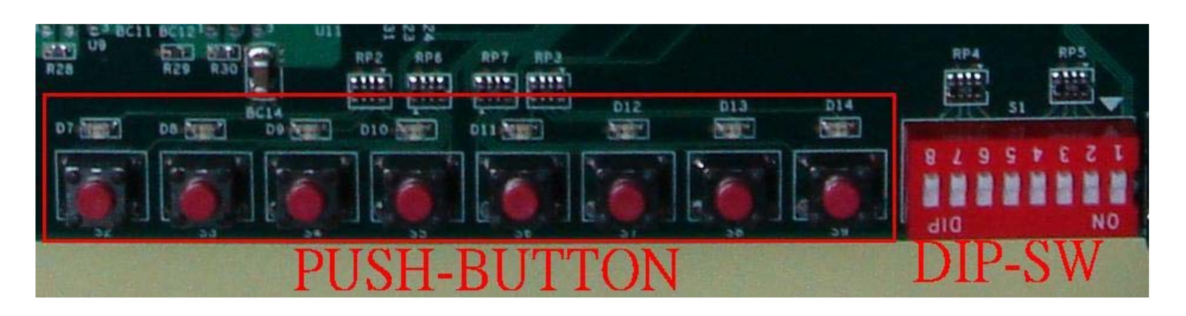
實驗板上有 8 個 PUSH_BUTTON 與八個 DIP_SWICTH,位於板子的最下方,
當 PUSH_BUTTON 按下時,輸入的電壓準位爲低電位’0’;當不按時爲’1’
當 DIP_SWITCH 往下切爲[ON]時,輸入電壓準位爲低電位’0’;而上切時爲[OFF].

```
NET "DIP_SWITCH<0>"    LOC = "P159"    ;
NET "DIP_SWITCH<1>"    LOC = "P169"    ;
NET "DIP_SWITCH<2>"    LOC = "P194"    ;
```

```
NET "DIP_SWITCH<3>"   LOC = "P204"   ;
NET "DIP_SWITCH<4>"   LOC = "P54"   ;
NET "DIP_SWITCH<5>"   LOC = "P91"   ;
NET "DIP_SWITCH<6>"   LOC = "P101"   ;
NET "DIP_SWITCH<7>"   LOC = "P58"   ;

NET "PUSH_BUTTON<7>"   LOC = "P154"   ;
NET "PUSH_BUTTON<6>"   LOC = "P148"   ;
NET "PUSH_BUTTON<5>"   LOC = "P142"   ;
NET "PUSH_BUTTON<4>"   LOC = "P136"   ;
NET "PUSH_BUTTON<3>"   LOC = "P130"   ;
NET "PUSH_BUTTON<2>"   LOC = "P124"   ;
NET "PUSH_BUTTON<1>"   LOC = "P118"   ;
NET "PUSH_BUTTON<0>"   LOC = "P110"   ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P110 | S2 | USER_SW8 | 按下時,輸入爲’0’ | |
| P118 | S3 | USER_SW7 | 按下時,輸入爲’0’ | |
| P124 | S4 | USER_SW6 | 按下時,輸入爲’0’ | |
| P130 | S5 | USER_SW5 | 按下時,輸入爲’0’ | |
| P136 | S6 | USER_SW4 | 按下時,輸入爲’0’ | |
| P142 | S7 | USER_SW3 | 按下時,輸入爲’0’ | |
| P148 | S8 | USER_SW2 | 按下時,輸入爲’0’ | |
| P154 | S9 | USER_SW1 | 按下時,輸入爲’0’ | |
| P159 | S1-1 | USER_DIP1 | | |
| P169 | S1-2 | USER_DIP2 | | |
| P194 | S1-3 | USER_DIP3 | | |
| P204 | S1-4 | USER_DIP4 | | |
| P54 | S1-5 | USER_DIP5 | | |
| P91 | S1-6 | USER_DIP6 | | |
| P101 | S1-7 | USER_DIP7 | | |
| P58 | S1-8 | USER_DIP8 | | |



## 2-5. LED 輸出

實驗板上有 8 個 LED 綠色 LED,當輸出高電位’1’時,LED 亮,
當輸出低電位’0’時,LED 不亮.

```
NET "LED<7>"   LOC = "P76"   ;
NET "LED<6>"   LOC = "P98"   ;
NET "LED<5>"   LOC = "P55"   ;
NET "LED<4>"   LOC = "P61"   ;
NET "LED<3>"   LOC = "P60"   ;
NET "LED<2>"   LOC = "P63"   ;
NET "LED<1>"   LOC = "P62"   ;
NET "LED<0>"   LOC = "P65"   ;
```

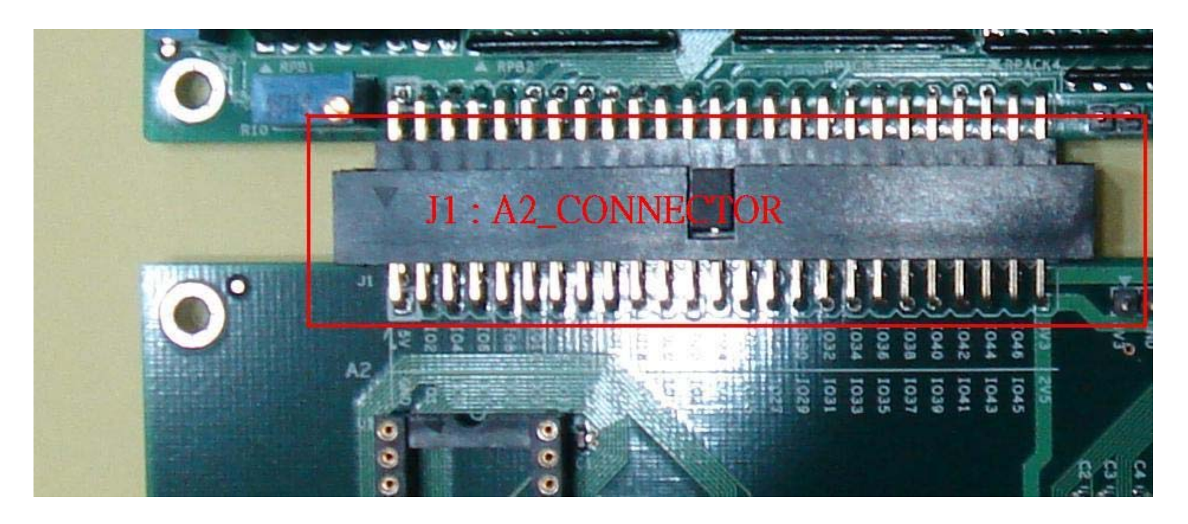
| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P65 | D7 | USER_LED1 | 輸出’1’→D7 亮起 | |
| P62 | D8 | USER_LED2 | 輸出’1’→D8 亮起 | |
| P63 | D9 | USER_LED3 | 輸出’1’→D9 亮起 | |
| P60 | D10 | USER_LED3 | 輸出’1’→D10 亮起 | |
| P61 | D11 | USER_LED4 | 輸出’1’→D11 亮起 | |
| P55 | D12 | USER_LED5 | 輸出’1’→D12 亮起 | |
| P98 | D13 | USER_LED6 | 輸出’1’→D13 亮起 | |
| P76 | D14 | USER_LED7 | 輸出’1’→D14 亮起 | |



## 2-6. J1 CONNECTOR (A2_CONNECTOR)

J1 提供 46 點輸出/輸入介面,提供板子擴充 IO 之用,其輸出準位爲標準的+3.3V 介面.

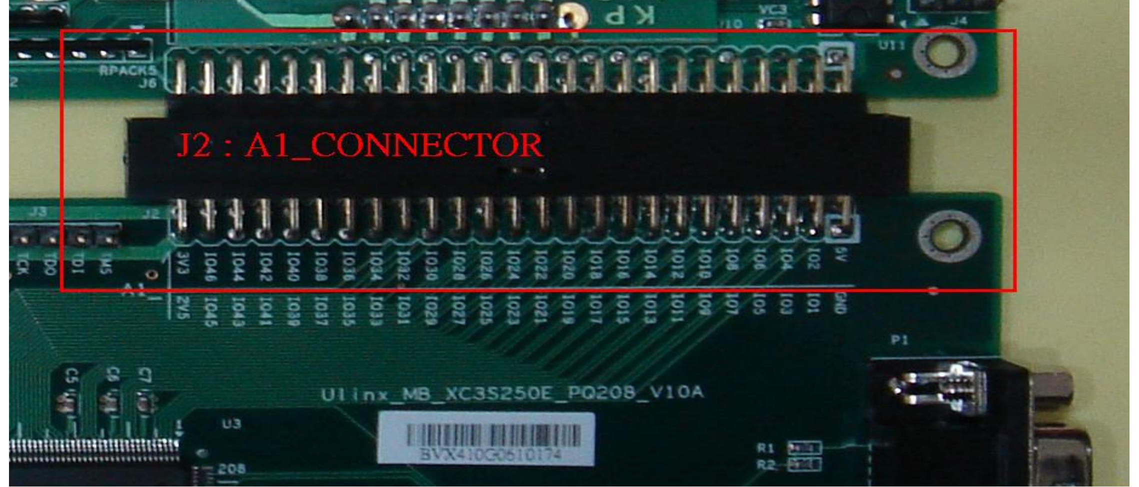
| Human_IO BOARD | FPGA PIN | SYMBOL | J1 | J1 | SYMBOL | FPGA PIN | Human_IO BOARD |
|---|---|---|---|---|---|---|---|
| | | GND | 1 | 2 | +5V | | |
| 7_SEG_A1 | P181 | A2_IO1 | 3 | 4 | A2_IO2 | P180 | 7_SEG_A2 |
| 7_SEG_A3 | P186 | A2_IO3 | 5 | 6 | A2_IO4 | P185 | 7_SEG_A4 |
| 7_SEG_A5 | P190 | A2_IO5 | 7 | 8 | A2_IO6 | P189 | 7_SEG_A6 |
| 7_SEG_A7 | P193 | A2_IO7 | 9 | 10 | A2_IO8 | P192 | 7_SEG_A8 |
| 7_SEG_CA | P197 | A2_IO9 | 11 | 12 | A2_IO10 | P196 | 7_SEG_CB |
| 7_SEG_CC | P200 | A2_IO11 | 13 | 14 | A2_IO12 | P199 | 7_SEG_CD |
| 7_SEG_CE | P203 | A2_IO13 | 15 | 16 | A2_IO14 | P202 | 7_SEG_CF |
| 7_SEG_CG | P206 | A2_IO15 | 17 | 18 | A2_IO16 | P205 | 7_SEG_DP |
| **LCD_RST** | P107 | A2_IO17 | 19 | 20 | A2_IO18 | P106 | **LCD_CS2** |
| **LCD_CS1** | P109 | A2_IO19 | 21 | 22 | A2_IO20 | P108 | **LCD_D7** |
| **LCD_D6** | P113 | A2_IO21 | 23 | 24 | A2_IO22 | P112 | **LCD_D5** |
| **LCD_D4** | P116 | A2_IO23 | 25 | 26 | A2_IO24 | P115 | **LCD_D3** |
| **LCD_D2** | P120 | A2_IO25 | 27 | 28 | A2_IO26 | P119 | **LCD_D1** |
| **LCD_D0** | P123 | A2_IO27 | 29 | 30 | A2_IO28 | P122 | **LCD_E** |
| **LCD_RW** | P127 | A2_IO29 | 31 | 32 | A2_IO30 | P126 | **LCD_IO** |
| PS2_CLK | P129 | A2_IO31 | 33 | 34 | A2_IO32 | P128 | PS2_DATA |
| USER_SW1 | P133 | A2_IO33 | 35 | 36 | A2_IO34 | P132 | USER_SW2 |
| USER_SW3 | P135 | A2_IO35 | 37 | 38 | A2_IO36 | P134 | USER_SW4 |
| **USER_DIP1** | P138 | A2_IO37 | 39 | 40 | A2_IO38 | P137 | **USER_DIP2** |
| **USER_DIP3** | P140 | A2_IO39 | 41 | 42 | A2_IO40 | P139 | **USER_DIP4** |
| ROT_IN1 | P145 | A2_IO41 | 43 | 44 | A2_IO42 | P144 | ROT_IN2 |
| ROT_IN3 | P147 | A2_IO43 | 45 | 46 | A2_IO44 | P146 | ROT_IN4 |
| IIC_SCL | P151 | A2_IO45 | 47 | 48 | A2_IO46 | P150 | IIC_SDA |
| | | +2.5V | 49 | 50 | +3.3V | | |



## 2-7. J2 CONNECTOR(A1_CONNECTOR

J2 提供 46 點輸出/輸入介面,提供板子擴充 IO 之用,其輸出準位爲標準的+3.3V 介面.

| Human_IO BOARD | FPGA PIN | SYMBOL | J2 | J2 | SYMBOL | FPGA PIN | Human_IO BOARD |
|---|---|---|---|---|---|---|---|
| | | GND | 1 | 2 | +5V | | |
| D16(綠色 LED) | P3 | A1_IO1 | 3 | 4 | A1_IO2 | P2 | D15(綠色 LED) |
| D14(綠色 LED) | P5 | A1_IO3 | 5 | 6 | A1_IO4 | P4 | D13(綠色 LED) |
| D12(綠色 LED) | P9 | A1_IO5 | 7 | 8 | A1_IO6 | P8 | D11(綠色 LED) |
| D10(綠色 LED) | P12 | A1_IO7 | 9 | 10 | A1_IO8 | P11 | D9 (綠色 LED) |
| D8 (紅色 LED) | P16 | A1_IO9 | 11 | 12 | A1_IO10 | P15 | D7 (紅色 LED) |
| D6 (紅色 LED) | P19 | A1_IO11 | 13 | 14 | A1_IO12 | P18 | D5 (紅色 LED) |
| D4 (紅色 LED) | P23 | A1_IO13 | 15 | 16 | A1_IO14 | P22 | D3 (紅色 LED) |
| D2 (紅色 LED) | P25 | A1_IO15 | 17 | 18 | A1_IO16 | P24 | D1 (紅色 LED) |
| KEY_IN4 | P29 | A1_IO17 | 19 | 20 | A1_IO18 | P28 | KEY_IN3 |
| KEY_IN2 | P31 | A1_IO19 | 21 | 22 | A1_IO20 | P30 | KEY_IN1 |
| KEY_OUT4 | P34 | A1_IO21 | 23 | 24 | A1_IO22 | P33 | KEY_OUT3 |
| KEY_OUT2 | P36 | A1_IO23 | 25 | 26 | A1_IO24 | P35 | KEY_OUT1 |
| EXT_OUT1 | P40 | A1_IO25 | 27 | 28 | A1_IO26 | P39 | EXT_OUT2 |
| EXT_OUT3 | P42 | A1_IO27 | 29 | 30 | A1_IO28 | P41 | EXT_OUT4 |
| EXT_IN1 | P48 | A1_IO29 | 31 | 32 | A1_IO30 | P47 | EXT_IN2 |
| EXT_IN3 | P50 | A1_IO31 | 33 | 34 | A1_IO32 | P49 | EXT_IN4 |
| ADC_CS | P187 | A1_IO33 | 35 | 36 | A1_IO34 | P179 | ADC_CLK |
| ADC_DO | P161 | A1_IO35 | 37 | 38 | A1_IO36 | P160 | ADC_DI |
| DAC_CS | P163 | A1_IO37 | 39 | 40 | A1_IO38 | P162 | DAC_CLK |
| DAC_DI | P165 | A1_IO39 | 41 | 42 | A1_IO40 | P164 | DAC_DO |
| VGA_VSYNC | P168 | A1_IO41 | 43 | 44 | A1_IO42 | P167 | VGA_HSYNC |
| VGA_B | P172 | A1_IO43 | 45 | 46 | A1_IO44 | P171 | VGA_G |
| VGA_R | P178 | A1_IO45 | 47 | 48 | A1_IO46 | P177 | DAC_CLR |
| | | +2.5V | 49 | 50 | +3.3V | | |

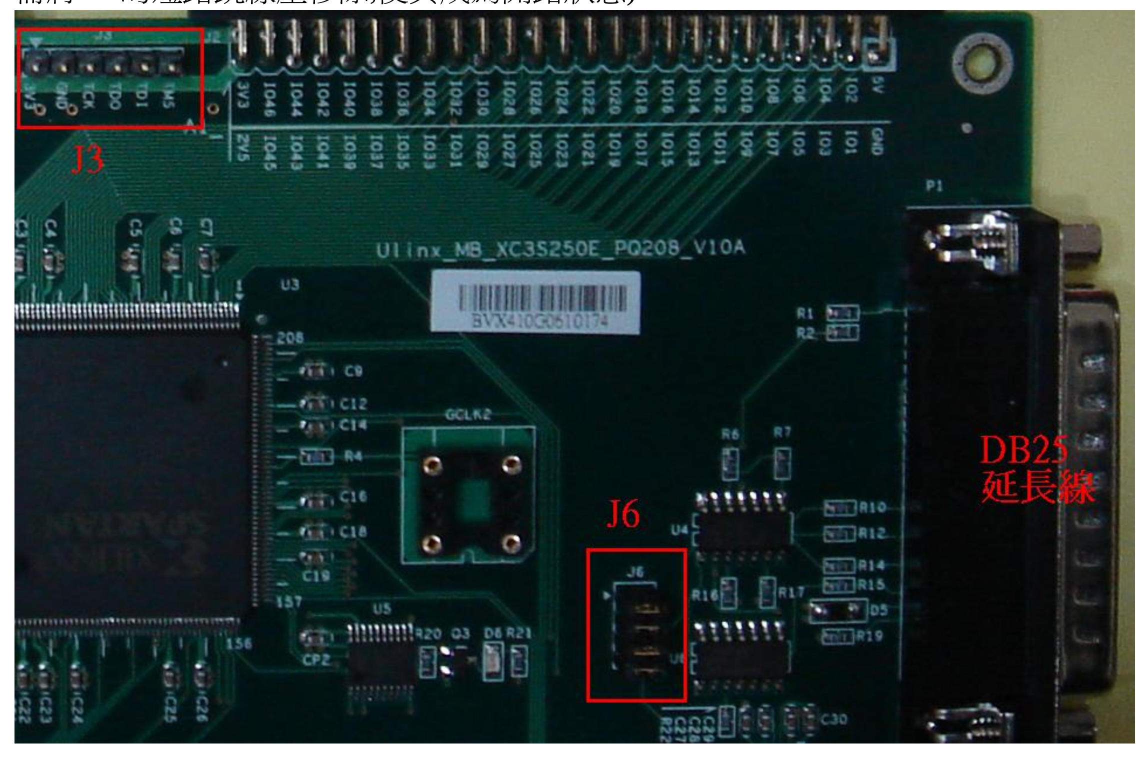


## 2-8. FPGA　Configuration

FPGA Configuration 提供使用者將自己設計的檔案輸入給 FPGA,而一般 FPGA 提供 2 種 Download 的方式,其一爲 JTAG,其一爲 Master Salve 兩種.

[第一種]: In_System Programming

透過 JTAG 與 ISE 軟體的 Impact,可以將使用者程式 Download 到 FPGA,這一種方式的介面相關電路已包含於板子之中,利用 DB25 的連接線,連接電腦的 Printer Port 與 Ulinx_MB_XC3S250E_PQ208 的 P1,就可以利用 Impact 來 Download.使用前請確認 J6 的 Connector 已經將 4 個短路跳線座裝好,如圖所示(若你想用現成 Parallel_Cable_III 或 Parallel_Cavle_IV 來 Download 的話,則可以利用 J3 來連接,但需將 J6 的短路跳線座移除,使其成爲開路狀態).

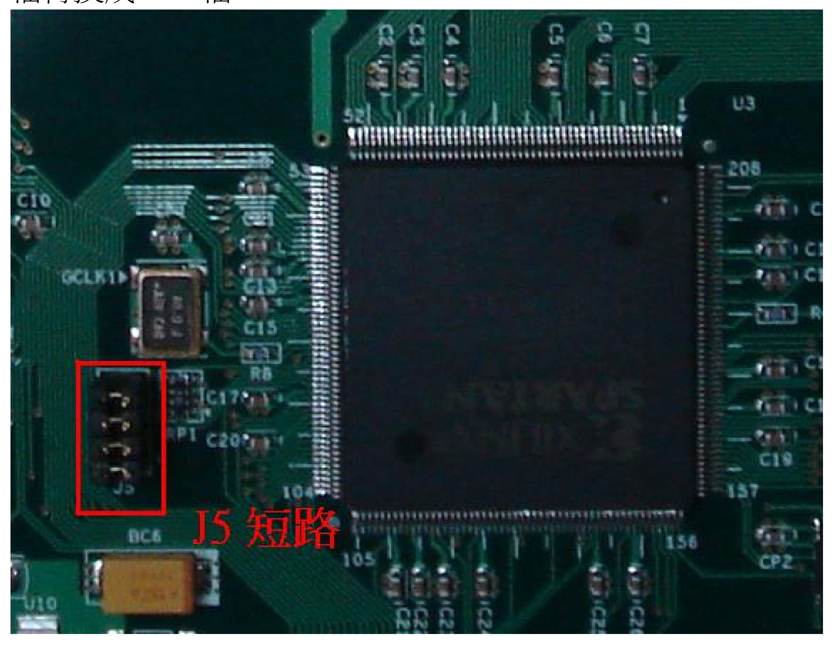


[第二種方式]: Master Slave

*Table 43:* **Spartan-3E Configuration Mode Options and Pin Settings**

| | Master Serial | SPI | BPI | Slave Parallel | Slave Serial | JTAG |
|---|---|---|---|---|---|---|
| M[2:0] mode pin settings | <0:0:0> | <0:0:1> | <0:1:0>=Up<br><0:1:1>=Down | <1:1:0> | <1:1:1> | <1:0:1> |
| Data width | Serial | Serial | Byte-wide | Byte-wide | Serial | Serial |
| Configuration memory source | Xilinx Platform Flash | Industry-standard SPI serial Flash | Industry-standard parallel NOR Flash or Xilinx parallel Platform Flash | Any source via microcontroller, CPU, Xilinx parallel Platform Flash, etc. | Any source via microcontroller, CPU, Xilinx Platform Flash, etc. | Any source via microcontroller, CPU, System ACE ™ CF, etc. |
| Clock source | Internal oscillator | Internal oscillator | Internal oscillator | External clock on CCLK pin | External clock on CCLK pin | External clock on TCK pin |
| Total I/O pins borrowed during configuration | 8 | 13 | 46 | 21 | 8 | 0 |
| Configuration mode for downstream daisy-chained FPGAs | Slave Serial | Slave Serial | Slave Parallel | Slave Parallel or Memory Mapped | Slave Serial | JTAG |
| Stand-alone FPGA applications (no external download host) | ✓ | ✓ | ✓ | Possible using XCFxxP Platform Flash, which optionally generates CCLK | Possible using XCFxxP Platform Flash, which optionally generates CCLK | |
| Uses low-cost, industry-standard Flash | | ✓ | ✓ | | | |
| Supports optional MultiBoot, multi-configuration mode | | | ✓ | | | |

這種方式,需將板子的 J5 以短路跳線座,將 J5 短路,而 JTAG 在 Download 時,需將 Bit 檔轉換成 mcs 檔.



## 2-9. FPGA

Ulinx_MB_XC3S250E_PQ208 爲 FPGA,使用 Xilinx 的 Sparatn3E 的 XC3S250E 元件,其包裝爲 PQ208,其相關接腳如表所示.

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P1 | | | PROG_B |
| P2 | A1_IO2 | O | IO_L01P_3 |
| P3 | A1_IO1 | O | IO_L01N_3 |
| P4 | A1_IO4 | O | IO_L02P_3 |
| P5 | A1_IO3 | O | IO_L02N_3/VREF_3 |
| P6 | | | IP |
| P7 | | | VCCAUX |
| P8 | A1_IO6 | O | IO_L03P_3 |
| P9 | A1_IO5 | O | IO_L03N_3 |
| P10 | | | GND |
| P11 | A1_IO8 | O | IO_L04P_3 |
| P12 | A1_IO7 | O | IO_L04N_3 |
| P13 | | | VCCINT |
| P14 | | | IP |
| P15 | A1_IO10 | O | IO_L05P_3 |
| P16 | A1_IO9 | O | IO_L05N_3 |
| P17 | | | GND |
| P18 | A1_IO12 | O | IO_L06P_3 |
| P19 | A1_IO11 | O | IO_L06N_3 |
| P20 | | I | IP/VREF_3 |
| P21 | | | VCCO_3 |
| P22 | A1_IO14 | O | IO_L07P_3/LHCLK0 |
| P23 | A1_IO13 | O | IO_L07N_3/LHCLK1 |
| P24 | A1_IO16 | O | IO_L08P_3/LHCLK2 |
| P25 | A1_IO15 | O | IO_L08N_3/LHCLK3/IRDY2 |
| P26 | | | IP |
| P27 | | | GND |
| P28 | A1_IO18 | I | IO_L09P_3/LHCLK4/TRDY2 |
| P29 | A1_IO17 | I | IO_L09N_3/LHCLK5 |
| P30 | A1_IO20 | I | IO_L10P_3/LHCLK6 |
| | | | |
| | | | |

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P31 | A1_IO19 | I | IO_L10N_3/LHCLK7 |
| P32 | | | IP |
| P33 | A1_IO22 | O | IO_L11P_3 |
| P34 | A1_IO21 | O | IO_L11N_3 |
| P35 | A1_IO24 | O | IO_L12P_3 |
| P36 | A1_IO23 | O | IO_L12N_3 |
| P37 | | | GND |
| P38 | | | VCCO_3 |
| P39 | A1_IO26 | | IO_L13P_3 |
| P40 | A1_IO25 | | IO_L13N_3 |
| P41 | A1_IO28 | | IO_L14P_3 |
| P42 | A1_IO27 | | IO_L14N_3 |
| P43 | | | IP |
| P44 | | | VCCAUX |
| P45 | RS232_TX | O | IO/VREF_3 |
| P46 | | | VCCO_3 |
| P47 | A1_IO30 | | IO_L15P_3 |
| P48 | A1_IO29 | | IO_L15N_3 |
| P49 | A1_IO32 | O | IO_L16P_3 |
| P50 | A1_IO31 | | IO_L16N_3 |
| P51 | | | IP |
| P52 | | | GND |
| P53 | | | GND |
| P54 | DIP_SWITCH_5 | I | IP |
| P55 | LED3 | O | IO_L01P_2/CSO_B |
| P56 | | | IO_L01N_2/INIT_B |
| P57 | | | IP_L02P_2 |
| P58 | DIP_SWITCH_8 | I | IP_L02N_2 |
| P59 | | | VCCO_2 |
| P60 | LED5 | O | IO_L03P_2/DOUT/BUSY |
| P61 | LED4 | O | IO_L03N_2/MOSI/CSI_B |
| P62 | LED6 | O | IO_L04P_2 |
| P63 | LED7 | O | IO_L04N_2 |
| P64 | | | IO_L05P_2 |
| | | | |
| | | | |

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P65 | LED8 | O | IO_L05N_2 |
| P66 | | | VCCAUX |
| P67 | | | VCCINT |
| P68 | | | IO_L06P_2 |
| P69 | | | IO_L06N_2 |
| P70 | | | GND |
| P71 | RS232_RX | I | IP_L07P_2 |
| P72 | | | IP_L07N_2/VREF_2 |
| P73 | | | VCCO_2 |
| P74 | | | IO_L08P_2/D7/GCLK12 |
| P75 | | | IO_L08N_2/D6/GCLK13 |
| P76 | LED1 | O | IO/D5 |
| P77 | | | IO_L09P_2/D4/GCLK14 |
| P78 | | | IO_L09N_2/D3/GCLK15 |
| P79 | | | GND |
| P80 | sys_clk_pin | I | IP_L10P_2/RDWR_B/GCLK0 |
| P81 | | | IP_L10N_2/M2/GCLK1 |
| P82 | | | IO_L11P_2/D2/GCLK2 |
| P83 | | | IO_L11N_2/D1/GCLK3 |
| P84 | | | IO/M1 |
| P85 | | | GND |
| P86 | | | IO_L12P_2/M0 |
| P87 | | | IO_L12N_2/DIN/D0 |
| P88 | | | VCCO_2 |
| P89 | | | IO_L13P_2 |
| P90 | | | IO_L13N_2 |
| P91 | DIP_SWITCH_6 | I | IP |
| P92 | | | VCCAUX |
| P93 | | | IO_L14P_2/A23 |
| P94 | | | IO_L14N_2/A22 |
| P95 | | | GND |
| P96 | | | IO_L15P_2/A21 |
| P97 | | | IO_L15N_2/A20 |
| P98 | LED2 | O | IO/VREF_2 |
| P99 | | | IO_L16P_2/VS2/A19 |
| P100 | | | IO_L16N_2/VS1/A18 |

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P101 | DIP_SWITCH_7 | I | IP |
| P102 | | | IO_L17P_2/VS0/A17 |
| P103 | | | IO_L17N_2/CCLK |
| P104 | | | DONE |
| P105 | | | GND |
| P106 | A2_IO18 | O | IO_L01P_1/A16 |
| P107 | A2_IO17 | O | IO_L01N_1/A15 |
| P108 | A2_IO20 | O | IO_L02P_1/A14 |
| P109 | A2_IO19 | O | IO_L02N_1/A13 |
| P110 | Push_Buttons_1( S2 ) | I | IP |
| P111 | | | VCCAUX |
| P112 | A2_IO22 | O | IO_L03P_1 |
| P113 | A2_IO21 | O | IO_L03N_1/VREF_1 |
| P114 | | | VCCO_1 |
| P115 | A2_IO24 | O | IO_L04P_1 |
| P116 | A2_IO23 | O | IO_L04N_1 |
| P117 | | | VCCINT |
| P118 | Push_Buttons_2( S3 ) | I | IP |
| P119 | A2_IO26 | O | IO_L05P_1/A12 |
| P120 | A2_IO25 | O | IO_L05N_1/A11 |
| P121 | | | GND |
| P122 | A2_IO28 | O | IO_L06P_1 |
| P123 | A2_IO27 | O | IO_L06N_1/VREF_1 |
| P124 | Push_Buttons_3( S4 ) | I | IP |
| P125 | | | VCCO_1 |
| P126 | A2_IO30 | O | IO_L07P_1/A10/RHCLK0 |
| P127 | A2_IO29 | O | IO_L07N_1/A9/RHCLK1 |
| P128 | A2_IO32 | O | IO_L08P_1/A8/RHCLK2 |
| P129 | A2_IO31 | O | IO_L08N_1/A7/RHCLK3/TRDY1 |
| P130 | Push_Buttons_4( S5 ) | I | IP |
| P131 | | | GND |
| P132 | A2_IO34 | I | IO_L09P_1/A6/RHCLK4/IRDY1 |
| P133 | A2_IO33 | I | IO_L09N_1/A5/RHCLK5 |
| P134 | A2_IO36 | I | IO_L10P_1/A4/RHCLK6 |
| P135 | A2_IO35 | I | IO_L10N_1/A3/RHCLK7 |
| P136 | Push_Buttons_5 ( S6 ) | I | IP/VREF_1 |

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P137 | A2_IO38 | I | IO_L11P_1/A2 |
| P138 | A2_IO37 | I | IO_L11N_1/A1 |
| P139 | A2_IO40 | I | IO_L12P_1 |
| P140 | A2_IO39 | I | IO_L12N_1/A0 |
| P141 | | | GND |
| P142 | Push_Buttons_6 ( S7 ) | I | IP |
| P143 | | | VCCO_1 |
| P144 | A2_IO42 | I | IO_L13P_1 |
| P145 | A2_IO41 | I | IO_L13N_1 |
| P146 | A2_IO44 | I | IO_L14P_1 |
| P147 | A2_IO43 | I | IO_L14N_1 |
| P148 | Push_Buttons_7( S8 ) | I | IP |
| P149 | | | VCCAUX |
| P150 | A2_IO46 | | IO_L15P_1/HDC |
| P151 | A2_IO45 | | IO_L15N_1/LDC0 |
| P152 | | | IO_L16P_1/LDC1 |
| P153 | | | IO_L16N_1/LDC2 |
| P154 | Push_Buttons_8( S9 ) | I | IP |
| P155 | TMS | | TMS |
| P156 | | | GND |
| P157 | TDO | | TDO |
| P158 | TCK | | TCK |
| P159 | DIP_Switches_1 | I | IP |
| P160 | A1_IO36 | | IO_L01P_0 |
| P161 | A1_IO35 | | IO_L01N_0 |
| P162 | A1_IO38 | | IO_L02P_0 |
| P163 | A1_IO37 | | IO_L02N_0/VREF_0 |
| P164 | A1_IO40 | | IO_L03P_0 |
| P165 | A1_IO39 | | IO_L03N_0 |
| P166 | | | VCCAUX |
| P167 | A1_IO42 | | IO_L04P_0 |
| P168 | A1_IO41 | | IO_L04N_0/VREF_0 |
| P169 | DIP_Switch_2 | I | IP |
| P170 | | | VCCINT |
| P171 | A1_IO44 | | IO_L05P_0 |
| P172 | A1_IO43 | | IO_L05N_0 |

| Pin No | Signal Name | I/O | FPGA Pin Name |
|---|---|---|---|
| P173 | | | GND |
| P174 | | | IP_L06P_0 |
| P175 | | | IP_L06N_0 |
| P176 | | | VCCO_0 |
| P177 | A1_IO46 | | IO_L07P_0/GCLK4 |
| P178 | A1_IO45 | | IO_L07N_0/GCLK5 |
| P179 | A1_IO34 | | IO/VREF_0 |
| P180 | A1_IO2 | O | IO_L08P_0/GCLK6 |
| P181 | A2_IO1 | O | IO_L08N_0/GCLK7 |
| P182 | | | GND |
| P183 | GCLK2 | | IP_L09P_0/GCLK8 |
| P184 | | | IP_L09N_0/GCLK9 |
| P185 | A2_IO4 | O | IO_L10P_0/GCLK10 |
| P186 | A2_IO3 | O | IO_L10N_0/GCLK11 |
| P187 | A1_IO33 | | IO |
| P188 | | | GND |
| P189 | A2_IO6 | O | IO_L11P_0 |
| P190 | A2_IO5 | O | IO_L11N_0 |
| P191 | | | VCCO_0 |
| P192 | A2_IO8 | O | IO_L12P_0 |
| P193 | A2_IO7 | O | IO_L12N_0/VREF_0 |
| P194 | DIP_Switches_3 | I | IP |
| P195 | | | VCCAUX |
| P196 | A2_IO10 | O | IO_L13P_0 |
| P197 | A2_IO9 | O | IO_L13N_0 |
| P198 | | | GND |
| P199 | A2_IO12 | O | IO_L14P_0 |
| P200 | A2_IO11 | O | IO_L14N_0/VREF_0 |
| P201 | | | VCCO_0 |
| P202 | A2_IO14 | O | IO_L15P_0 |
| P203 | A2_IO13 | O | IO_L15N_0 |
| P204 | DIP_Switches_4 | I | IP |
| P205 | A2_IO16 | O | IO_L16P_0 |
| P206 | A2_IO15 | O | IO_L16N_0/HSWAP |
| P207 | TDI | | TDI |
| P208 | | | GND |

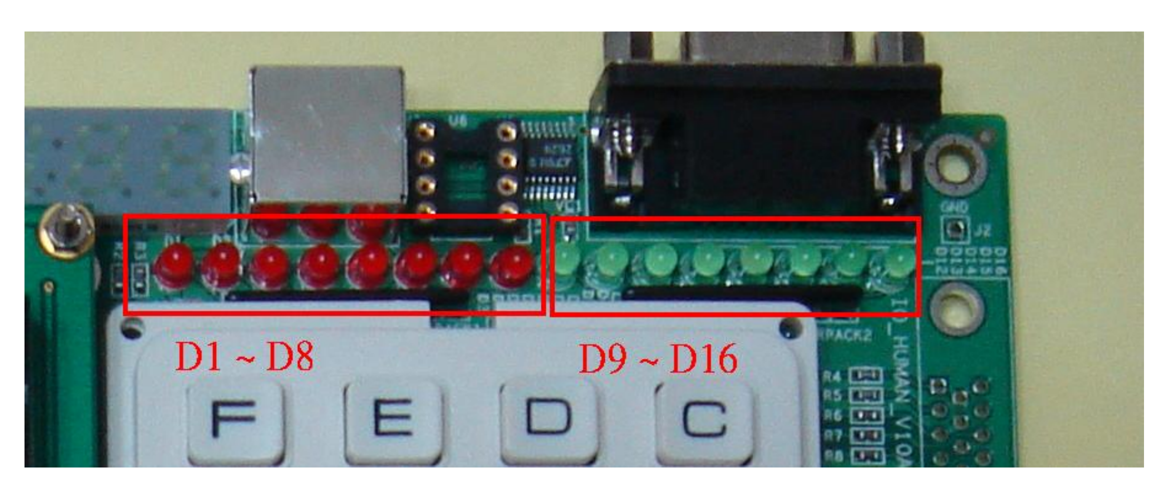
# 第三章 ：Human_IO

Human_IO 為 MB_XC3S250E 的擴充板,包含液晶介面,鍵盤,LED…等週邊介面,再利用 J5,J6 連接 MB_XC3S250E 的 J1,J2,本章節主要是敘述 HUMAIN_IO 相關週邊電路的相關說明.

## 3-1. IO_LED16

Human_IO 共有 16 個 LED,其中 8 顆為綠色,8 顆為紅色,
當 FPGA 輸出邏輯’1’(High)時,LED 亮.
當 FPGA 輸出邏輯’0’(LOW)時,LED 暗.

```
NET "IO_LED16<0>"     LOC = "P3"    ;
NET "IO_LED16<1>"     LOC = "P2"    ;
NET "IO_LED16<2>"     LOC = "P5"    ;
NET "IO_LED16<3>"     LOC = "P4"    ;
NET "IO_LED16<4>"     LOC = "P9"    ;
NET "IO_LED16<5>"     LOC = "P8"    ;
NET "IO_LED16<6>"     LOC = "P12"   ;
NET "IO_LED16<7>"     LOC = "P11"   ;
NET "IO_LED16<8>"     LOC = "P16"   ;
NET "IO_LED16<9>"     LOC = "P15"   ;
NET "IO_LED16<10>"    LOC = "P19"   ;
NET "IO_LED16<11>"    LOC = "P18"   ;
NET "IO_LED16<12>"    LOC = "P23"   ;
NET "IO_LED16<13>"    LOC = "P22"   ;
NET "IO_LED16<14>"    LOC = "P25"   ;
NET "IO_LED16<15>"    LOC = "P24"   ;
```



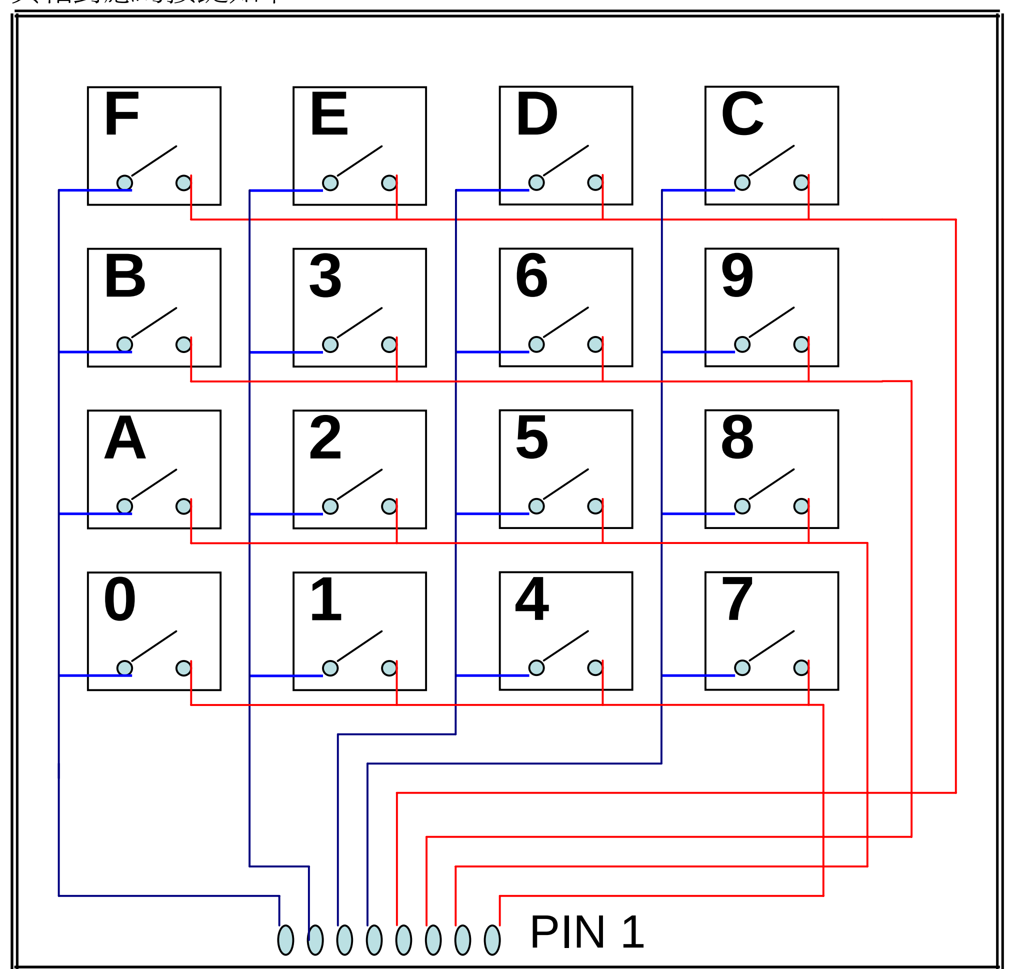
| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P3 | A1_IO1 | D16 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P2 | A1_IO2 | D15 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P5 | A1_IO3 | D14 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P4 | A1_IO4 | D13 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P9 | A1_IO5 | D12 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P8 | A1_IO6 | D11 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P12 | A1_IO7 | D10 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P11 | A1_IO8 | D9 | FPGA 輸出’1’,LED 亮 | 綠色 LED |
| P16 | A1_IO9 | D8 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P15 | A1_IO10 | D7 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P19 | A1_IO11 | D6 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P18 | A1_IO12 | D5 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P23 | A1_IO13 | D4 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P22 | A1_IO14 | D3 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P25 | A1_IO15 | D2 | FPGA 輸出’1’,LED 亮 | 紅色 LED |
| P24 | A1_IO16 | D1 | FPGA 輸出’1’,LED 亮 | 紅色 LED |

## 3-2. IO_KEY4X4

Human_IO 有一個 4X4 的鍵盤,共可定義 16 個按鍵,4X4 按鍵可以以掃描方式控制.

```
NET "IO_KEYI<3>"     LOC = "P29"   ;
NET "IO_KEYI<2>"     LOC = "P28"   ;
NET "IO_KEYI<1>"     LOC = "P31"   ;
NET "IO_KEYI<0>"     LOC = "P30"   ;
NET "IO_KEYO<3>"     LOC = "P34"   ;
NET "IO_KEYO<2>"     LOC = "P33"   ;
NET "IO_KEYO<1>"     LOC = "P36"   ;
NET "IO_KEYO<0>"     LOC = "P35"   ;
```

其相對應的按鍵如下.



| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P35 | A1_IO24 | KEY4X4_PIN1 | 列 1 | 綠色 LED |
| P36 | A1_IO23 | KEY4X4_PIN2 | 列 2 | 綠色 LED |
| P33 | A1_IO22 | KEY4X4_PIN3 | 列 3 | 綠色 LED |
| P34 | A1_IO21 | KEY4X4_PIN4 | 列 4 | 綠色 LED |
| P30 | A1_IO20 | KEY4X4_PIN5 | 行 1 | 紅色 LED |
| P31 | A1_IO19 | KEY4X4_PIN6 | 行 2 | 紅色 LED |
| P28 | A1_IO18 | KEY4X4_PIN7 | 行 3 | 紅色 LED |
| P29 | A1_IO17 | KEY4X4_PIN8 | 行 4 | 紅色 LED |

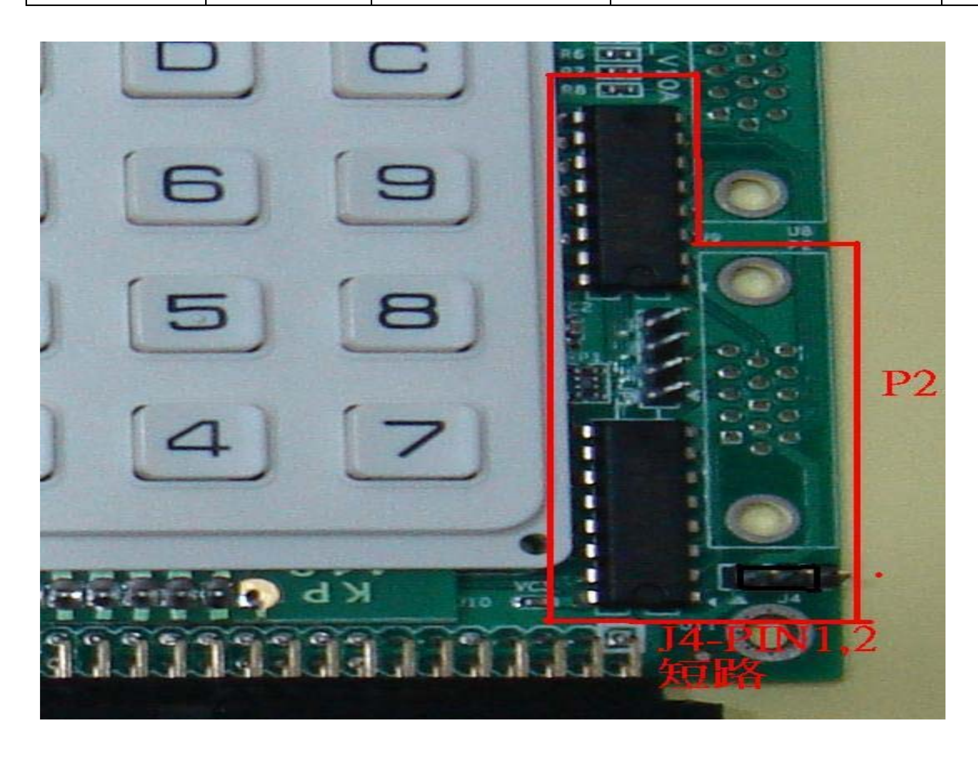


# 3-3. DIFFERENTIAL LINE RECEVIER & LINE DRIVER

Human_IO 有一個 4 個 Differential Line Driver 與 4 個 Differential Line Receiver, 可以提供 Differential 的介面.透過 P2 與 JP1,可以提供與其它介面的連接之用.
請注意需將 JP1 的 PIN1 與 PIN2 短路

```
NET "IO_MC3487_O<0>"        LOC = "P40"   ;
NET "IO_MC3487_O<1>"        LOC = "P39"   ;
NET "IO_MC3487_O<2>"        LOC = "P42"   ;
NET "IO_MC3487_O<3>"        LOC = "P41"   ;
NET "IO_MC3486_I<0>"        LOC = "P48"   ;
NET "IO_MC3486_I<1>"        LOC = "P47"   ;
NET "IO_MC3486_I<2>"        LOC = "P50"   ;
NET "IO_MC3486_I<3>"        LOC = "P49"   ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P40 | A1_IO25 | DIFF OUT1 | TTL DIFF OUT(5V) | P2 的 PIN1,2 |
| P39 | A1_IO26 | DIFF OUT2 | TTL DIFF OUT | P2 的 PIN3,4 |
| P42 | A1_IO27 | DIFF OUT3 | TTL DIFF OUT | P2 的 PIN5,6 |
| P41 | A1_IO28 | DIFF OUT4 | TTL DIFF OUT | JP1 的 PIN1,2 |
| P48 | A1_IO29 | DIFF IN1 | TTL DIFF IN(5V) | P2 的 PIN9,10 |
| P47 | A1_IO30 | DIFF IN2 | TTL DIFF IN | P2 的 PIN11,12 |
| P50 | A1_IO31 | DIFF IN3 | TTL DIFF IN | P2 的 PIN13,14 |
| P49 | A1_IO32 | DIFF IN4 | TTL DIFF IN | JP1 的 PIN3,4 |



## 3-4. ANALOG IN / ANALOG OUT

Human_IO 有 2 頻道 8 位元類比輸入與 4 個頻道 12 位元類比輸出,ADC 的元件爲 ADC0832,而 DAC 的元件則爲 LTC2624,其規格如下:

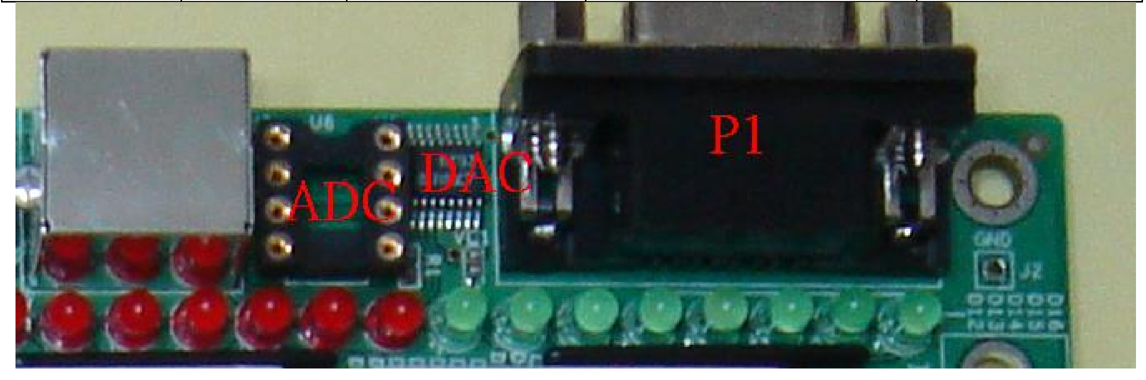
ADC1:由 P1 的 PIN7 輸入,輸入的電壓範圍爲 0~5V,轉換時間爲 32us,解析度爲 8 位元
ADC2:由 P1 的 PIN8 輸入,輸入的電壓範圍爲 0~5V,轉換時間爲 32us,解析度爲 8 位元
DAC1:由 P1 的 PIN1 輸出,輸出的電壓準位爲 0~3.3V,解析度 12 位元
DAC2:由 P1 的 PIN2 輸出,輸出的電壓準位爲 0~3.3V,解析度 12 位元
DAC3:由 P1 的 PIN3 輸出,輸出的電壓準位爲 0~3.3V,解析度 12 位元
DAC4:由 P1 的 PIN4 輸出,輸出的電壓準位爲 0~3.3V,解析度 12 位元

ADC 與 DAC 是透過串列方式控制,其轉換時間與轉換時序,由 FPGA 產生.

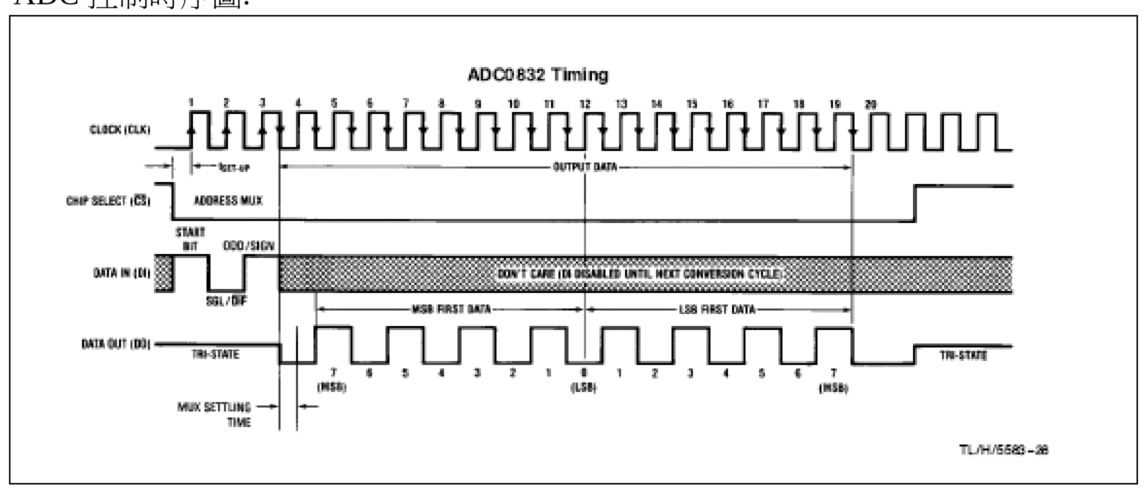
```
NET "IO_ADC_CSN"        LOC = "P187"  ;
NET "IO_ADC_CLK"        LOC = "P179"  ;
NET "IO_ADC_SDI"        LOC = "P135"  ;
NET "IO_ADC_SDO"        LOC = "P160"  ;

NET "IO_DAC_CS"         LOC = "P163"  ;
NET "IO_DAC_SCK"        LOC = "P162"  ;
NET "IO_DAC_SDI"        LOC = "P165"  ;
NET "IO_DAC_SDO"        LOC = "P164"  ;
NET "IO_DAC_CLR"        LOC = "P177"  ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P187 | A1_IO33 | ADC_CSN | ADC_CSN OUTPUT | |
| P179 | A1_IO34 | ADC_CLK | ADC_CLK OUTPUT | |
| P135 | A1_IO35 | ADC_SDI | ADC_SDI INPUT | |
| P160 | A1_IO36 | ADC_SDO | ADC_SDO INPUT | |
| P163 | A1_IO37 | DAC_CS | DAC_CS OUTPUT | |
| P162 | A1_IO38 | DAC_SCK | DAC_SCK OUTPUT | |
| P165 | A1_IO39 | DAC_SDI | DAC_SDI OUTPUT | |
| P164 | A1_IO40 | DAC_SDO | DAC_SDO OUTPUT | |
| P177 | A1_IO46 | DAC_CLR | DAC_CLR OUTOUT | |



ADC 控制時序圖.




DAC 控制時序圖.

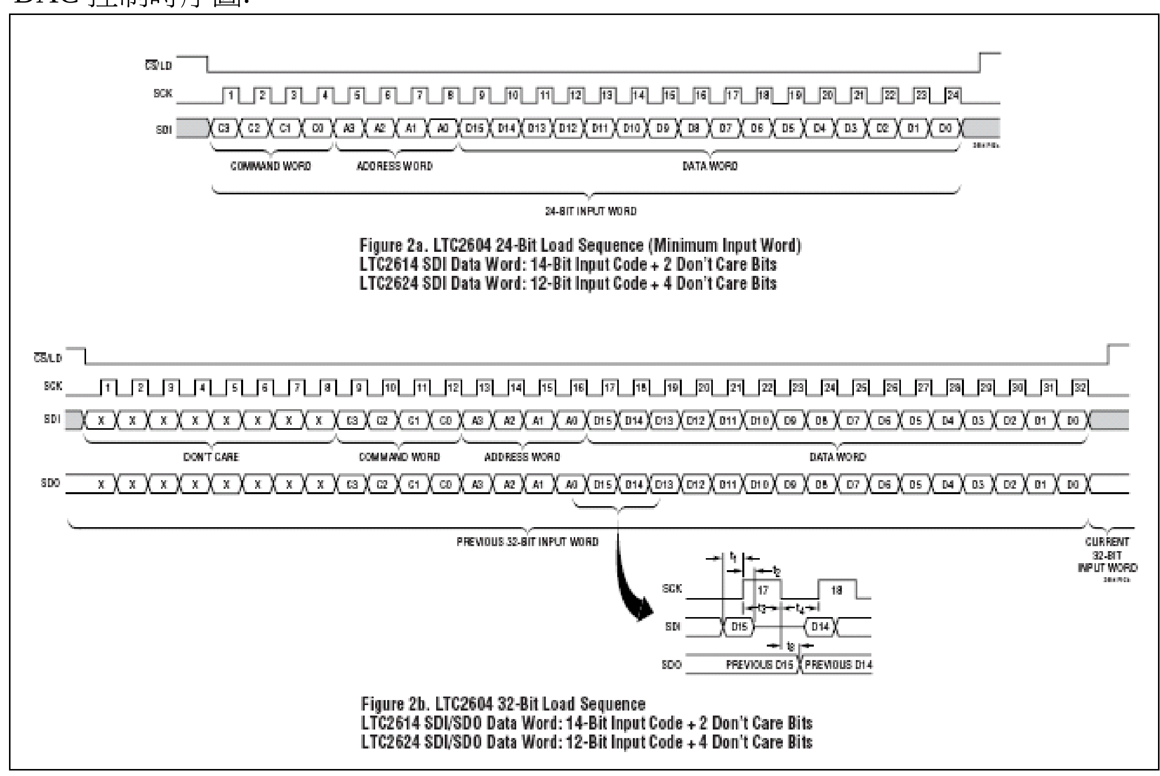
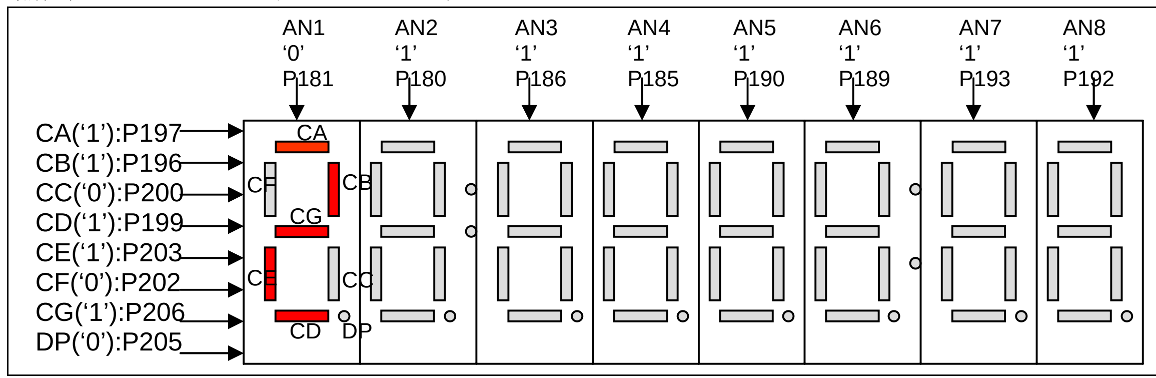



Figure 2a. LTC2604 24-Bit Load Sequence (Minimum Input Word)
LTC2614 SDI Data Word: 14-Bit Input Code + 2 Don't Care Bits
LTC2624 SDI Data Word: 12-Bit Input Code + 4 Don't Care Bits

Figure 2b. LTC2604 32-Bit Load Sequence
LTC2614 SDI/SDO Data Word: 14-Bit Input Code + 2 Don't Care Bits
LTC2624 SDI/SDO Data Word: 12-Bit Input Code + 4 Don't Care Bits

# 3-5. 七節燈管

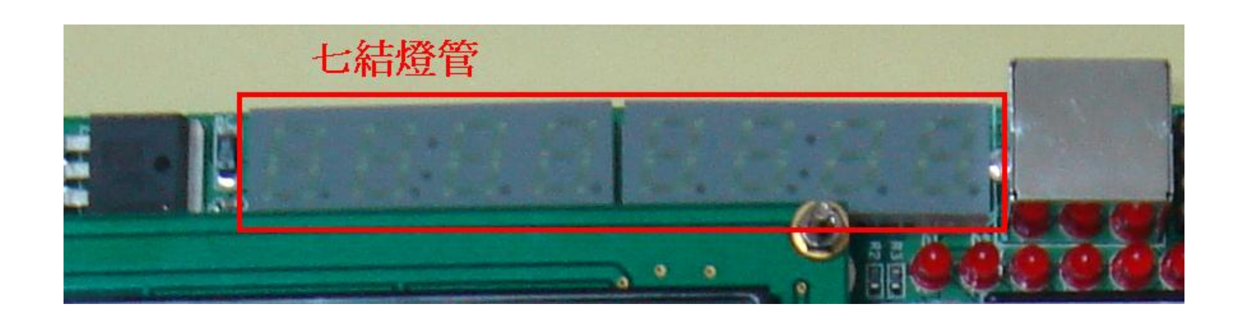
Human_IO 提供 8 個七節燈管,由 FPGA 控制.其控制方法為掃描式,如圖所示,若要控制左邊第一個七節燈管輸出’2’的字型,可以先輸出”11011010”到 CA~DP,然後輸出”01111111”到 AN1~AN8 即可.




```
NET "IO_DIGIT<0>"      LOC = "P181"   ;   ##AN1
NET "IO_DIGIT<1>"      LOC = "P180"   ;   ##AN2
NET "IO_DIGIT<2>"      LOC = "P186"   ;   ##AN3
NET "IO_DIGIT<3>"      LOC = "P185"   ;   ##AN4
NET "IO_DIGIT<4>"      LOC = "P190"   ;   ##AN5
NET "IO_DIGIT<5>"      LOC = "P189"   ;   ##AN6
NET "IO_DIGIT<6>"      LOC = "P193"   ;   ##AN7
NET "IO_DIGIT<7>"      LOC = "P192"   ;   ##AN8

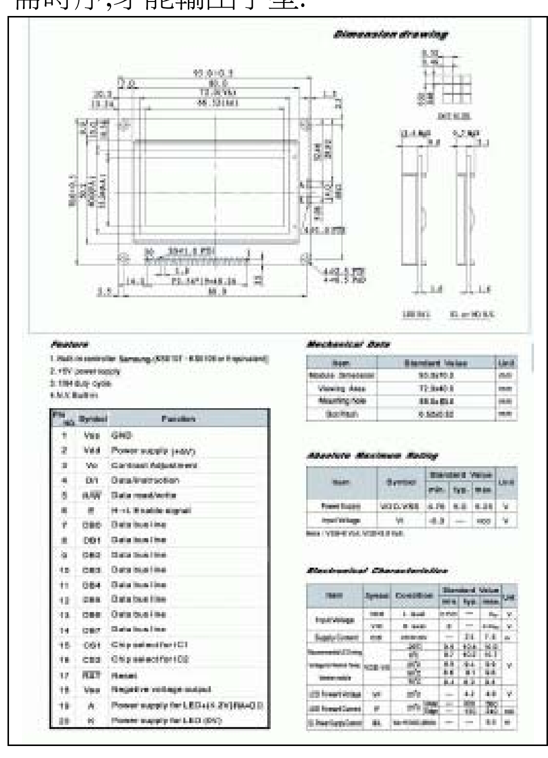
NET "IO_SEGMENT<0>"   LOC = "P197"   ;   ##CA
NET "IO_SEGMENT<1>"   LOC = "P196"   ;   ##CB
NET "IO_SEGMENT<2>"   LOC = "P200"   ;   ##CC
NET "IO_SEGMENT<3>"   LOC = "P199"   ;   ##CD
NET "IO_SEGMENT<4>"   LOC = "P203"   ;   ##CE
NET "IO_SEGMENT<5>"   LOC = "P202"   ;   ##CF
NET "IO_SEGMENT<6>"   LOC = "P206"   ;   ##CG
NET "IO_SEGMENT<7>"   LOC = "P205"   ;   ##DP
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P181 | A2_IO1 | IO_DIGIT<0> | 輸出'0',動作 | AN1 |
| P180 | A2_IO2 | IO_DIGIT<1> | 輸出'0',動作 | AN2 |
| P186 | A2_IO3 | IO_DIGIT<2> | 輸出'0',動作 | AN3 |
| P185 | A2_IO4 | IO_DIGIT<3> | 輸出'0',動作 | AN4 |
| P190 | A2_IO5 | IO_DIGIT<4> | 輸出'0',動作 | AN5 |
| P189 | A2_IO6 | IO_DIGIT<5> | 輸出'0',動作 | AN6 |
| P193 | A2_IO7 | IO_DIGIT<6> | 輸出'0',動作 | AN7 |
| P192 | A2_IO8 | IO_DIGIT<7> | 輸出'0',動作 | AN8 |
| P197 | A2_IO9 | IO_SEGEMENT<0> | 輸出'1',動作 | U4 的 CA |
| P196 | A2_IO10 | IO_SEGEMENT<1> | 輸出'1',動作 | U4 的 CB |
| P200 | A2_IO11 | IO_SEGEMENT<2> | 輸出'1',動作 | U4 的 CC |
| P199 | A2_IO12 | IO_SEGEMENT<3> | 輸出'1',動作 | U4 的 CD |
| P203 | A2_IO13 | IO_SEGEMENT<4> | 輸出'1',動作 | U4 的 CE |
| P202 | A2_IO14 | IO_SEGEMENT<5> | 輸出'1',動作 | U4 的 CF |
| P206 | A2_IO15 | IO_SEGEMENT<6> | 輸出'1',動作 | U4 的 CG |
| P205 | A2_IO16 | IO_SEGEMENT<7> | 輸出'1',動作 | U4 的 DP |



# 3-6. LCD128X64

LCD128X64 是一個 128 X 64 PIXEL 的液晶顯示器,可以顯示圖形式的圖案,包含中文字的字型,LCD128X64 並未提供已建好的字型,使用者需自行建立字型,並配合所需時序,才能輸出字型.



| Pin NO. | Symbol | Function |
|---|---|---|
| 1 | Vss | GND |
| 2 | Vdd | Power supply (+5V) |
| 3 | Vo | Contrast Adjustment |
| 4 | D/I | Data/Instruction |
| 5 | R/W | Data read/write |
| 6 | E | H→L Enable signal |
| 7 | DB0 | Data bus line |
| 8 | DB1 | Data bus line |
| 9 | DB2 | Data bus line |
| 10 | DB3 | Data bus line |
| 11 | DB4 | Data bus line |
| 12 | DB5 | Data bus line |
| 13 | DB6 | Data bus line |
| 14 | DB7 | Data bus line |
| 15 | CS1 | Chip select for IC1 |
| 16 | CS2 | Chip select for IC2 |
| 17 | RST | Reset |
| 18 | Vee | Negative voltage output |
| 19 | A | Power supply for LED+ |
| 20 | K | Power supply for LED (0V) |

```
Net "IO_LCD128x64<0>"    LOC = "P123" ;    ##LCD_DO(A2_IO27)
Net "IO_LCD128x64<1>"    LOC = "P119" ;    ##LCD_D1(A2_IO26)
Net "IO_LCD128x64<2>"    LOC = "P120" ;    ##LCD_D2(A2_IO25)
Net "IO_LCD128x64<3>"    LOC = "P115" ;    ##LCD_D3(A2_IO24)
Net "IO_LCD128x64<4>"    LOC = "P116" ;    ##LCD_D4(A2_IO23)
Net "IO_LCD128x64<5>"    LOC = "P112" ;    ##LCD_D5(A2_IO22)
Net "IO_LCD128x64<6>"    LOC = "P113" ;    ##LCD_D6(A2_IO21)
Net "IO_LCD128x64<7>"    LOC = "P108" ;    ##LCD_D7(A2_IO20)

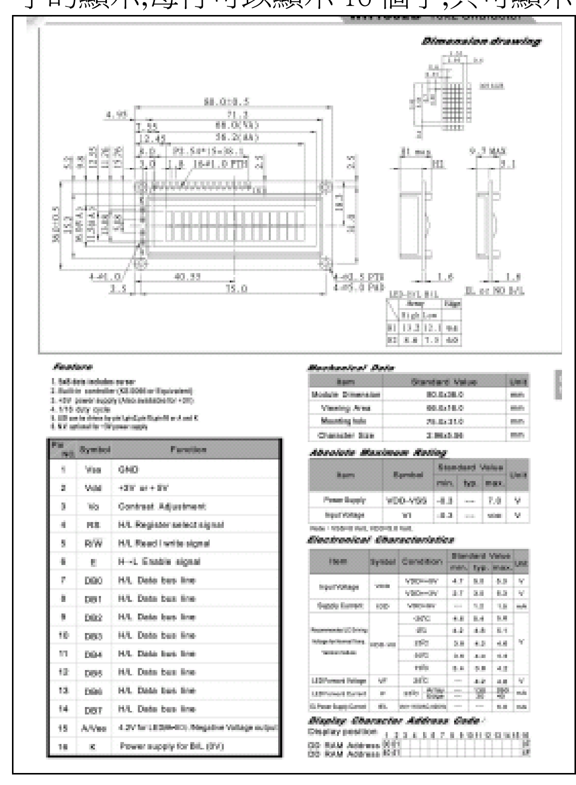
Net "IO_LCD128x64<10>"    LOC = "P107" ;    ##LCD_RST(A2_IO17)
Net "IO_LCD128x64<11>"    LOC = "P106" ;    ##LCD_CS2(A2_IO18)
Net "IO_LCD128x64<12>"    LOC = "P109" ;    ##LCD_CS1(A2_IO19)
Net "IO_LCD128x64<13>"    LOC = "P122" ;    ##LCD_E (A2_IO28)
Net "IO_LCD128x64<14>"    LOC = "P127" ;    ##LCD_RW(A2_IO29)
Net "IO_LCD128x64<15>"    LOC = "P126" ;    ##LCD_DI(A2_IO30)
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P123 | A2_IO27 | IO_LCD128X64<0> | FPGA_LCD_D0 | U13_PIN7 |
| P119 | A2_IO26 | IO_ LCD128X64<1> | FPGA_LCD_D1 | U13_PIN8 |
| P120 | A2_IO25 | IO_ LCD128X64<2> | FPGA_LCD_D2 | U13_PIN9 |
| P115 | A2_IO24 | IO_ LCD128X64<3> | FPGA_LCD_D3 | U13_PIN10 |
| P116 | A2_IO23 | IO_ LCD128X64<4> | FPGA_LCD_D4 | U13_PIN11 |
| P112 | A2_IO22 | IO_ LCD128X64<5> | FPGA_LCD_D5 | U13_PIN12 |
| P113 | A2_IO21 | IO_ LCD128X64<6> | FPGA_LCD_D6 | U13_PIN13 |
| P108 | A2_IO20 | IO_ LCD128X64<7> | FPGA_LCD_D7 | U13_PIN14 |
| P107 | A2_IO17 | IO_ LCD128X64<10> | FPGA_LCD_RST | U13_PIN17 |
| P106 | A2_IO18 | IO_ LCD128X64<11> | FPGA_LCD_CS2 | U13_PIN16 |
| P109 | A2_IO19 | IO_ LCD128X64<12> | FPGA_LCD_CS1 | U13_PIN15 |
| P122 | A2_IO28 | IO_ LCD128X64<13> | FPGA_LCD_E | U13_PIN6 |
| P127 | A2_IO29 | IO_ LCD128X64<14> | FPGA_LCD_RW | U13_PIN5 |
| P126 | A2_IO30 | IO_ LCD128X64<15> | FPGA_LCD_DI | U13_PIN4 |



## 3-7. LCD16X2

LCD16X2 是一個文字型的液晶顯示器,已內建 ASCII 字型於 LCD16X2 內,提供文字的顯示,每行可以顯示 16 個字,共可顯示兩行.




| Pin NO. | Symbol | Function |
|---|---|---|
| 1 | Vss | GND |
| 2 | Vdd | +3V or +5V |
| 3 | Vo | Contrast Adjustment |
| 4 | RS | H/L Register select signal |
| 5 | R/W | H/L Read / write signal |
| 6 | E | H→L Enable signal |
| 7 | DB0 | H/L Data bus line |
| 8 | DB1 | H/L Data bus line |
| 9 | DB2 | H/L Data bus line |
| 10 | DB3 | H/L Data bus line |
| 11 | DB4 | H/L Data bus line |
| 12 | DB5 | H/L Data bus line |
| 13 | DB6 | H/L Data bus line |
| 14 | DB7 | H/L Data bus line |
| 15 | A/Vee | 4.2V for LED / Negative Voltage output |
| 16 | K | Power supply for B/L (0V) |

| Item | Standard Value | Unit |
|---|---|---|
| Module Dimension | 80.0x36.0 | mm |
| Viewing Area | 66.0x16.0 | mm |
| Mounting hole | 75.0x31.0 | mm |
| Character Size | [illegible] | mm |

| Item | Symbol | Standard Value min. | typ. | max. | Unit |
|---|---|---|---|---|---|
| Power Supply | VDD-VSS | -0.3 | — | 7.0 | V |
| Input Voltage | VI | -0.3 | — | vdd | V |

```
Net "IO_LCD16x2<0>"    LOC = "P123" ;    ##LCD_DO(A2_IO27)
Net "IO_LCD16x2<1>"    LOC = "P119" ;    ##LCD_D1(A2_IO26)
Net "IO_LCD16x2<2>"    LOC = "P120" ;    ##LCD_D2(A2_IO25)
Net "IO_LCD16x2<3>"    LOC = "P115" ;    ##LCD_D3(A2_IO24)
Net "IO_LCD16x2<4>"    LOC = "P116" ;    ##LCD_D4(A2_IO23)
Net "IO_LCD16x2<5>"    LOC = "P112" ;    ##LCD_D5(A2_IO22)
Net "IO_LCD16x2<6>"    LOC = "P113" ;    ##LCD_D6(A2_IO21)
Net "IO_LCD16x2<7>"    LOC = "P108" ;    ##LCD_D7(A2_IO20)

Net "IO_LCD16x2<13>"    LOC = "P122" ;    ##LCD_E (A2_IO28)
Net "IO_LCD16x2<14>"    LOC = "P127" ;    ##LCD_RW(A2_IO29)
Net "IO_LCD16x2<15>"    LOC = "P126" ;    ##LCD_DI(A2_IO30)
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P123 | A2_IO27 | IO_LCD16X2<0> | FPGA_LCD_D0 | U12_PIN7 |
| P119 | A2_IO26 | IO_ LCD16X2<1> | FPGA_LCD_D1 | U12_PIN8 |
| P120 | A2_IO25 | IO_ LCD16X2<2> | FPGA_LCD_D2 | U12_PIN9 |
| P115 | A2_IO24 | IO_ LCD16X2<3> | FPGA_LCD_D3 | U12_PIN10 |
| P116 | A2_IO23 | IO_ LCD16X2<4> | FPGA_LCD_D4 | U12_PIN11 |
| P112 | A2_IO22 | IO_ LCD16X2<5> | FPGA_LCD_D5 | U12_PIN12 |
| P113 | A2_IO21 | IO_ LCD16X2<6> | FPGA_LCD_D6 | U12_PIN13 |
| P108 | A2_IO20 | IO_ LCD16X2<7> | FPGA_LCD_D7 | U12_PIN14 |
| P122 | A2_IO28 | IO_ LCD16X2<13> | FPGA_LCD_E | U12_PIN6 |
| P127 | A2_IO29 | IO_ LCD16X2<14> | FPGA_LCD_RW | U12_PIN5 |
| P126 | A2_IO30 | IO_ LCD16X2<15> | FPGA_LCD_DI | U12_PIN4 |

# 3-8. PS2

PS2 提供 PC 個人電腦的鍵盤介面.

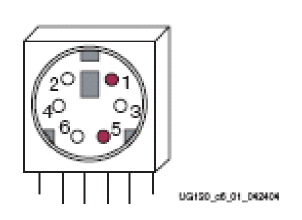


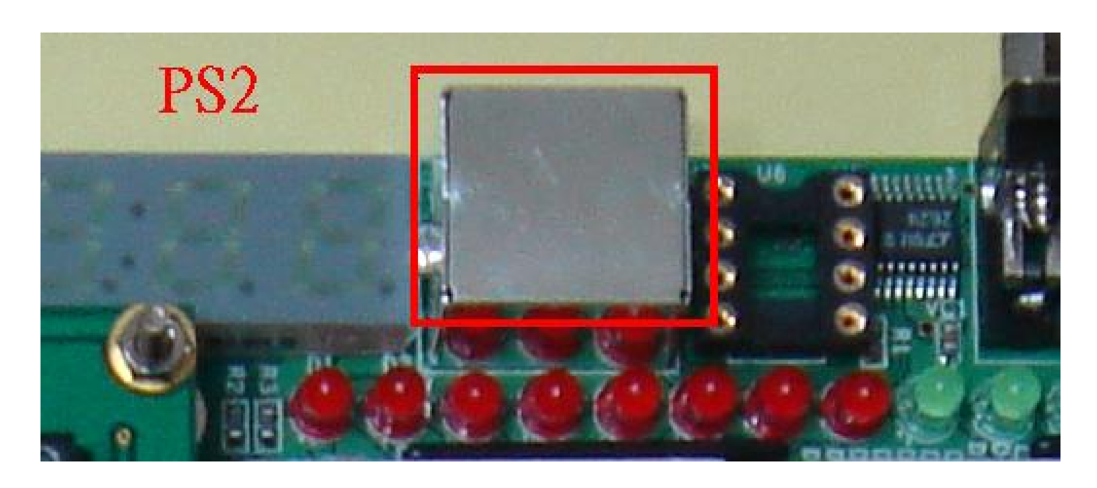

*Figure 6-1:* **PS/2 DIN Connect**

*Table 6-1:* **PS/2 Connections to the Spartan-3 FPGA**

| PS/2 DIN Pin | Signal |
|---|---|
| 1 | DATA (PS2D) |
| 2 | Reserved |
| 3 | GND |
| 4 | Voltage Supply |
| 5 | CLK (PS2C) |
| 6 | Reserved |

```
Net "IO_PS2_DATA"    LOC = "P129" ;    ##A2_IO31
Net "IO_PS2_CLK"      LOC = "P128" ;    ##A2_IO32
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P129 | A2_IO31 | PS2_DATA | | U3_PIN1 |
| P128 | A2_IO32 | PS2_CLK | | U3_PIN5 |



## 3-9. VGA

PS2 提供 PC 個人電腦的 VGA 介面,但只支援 8 種顏色.

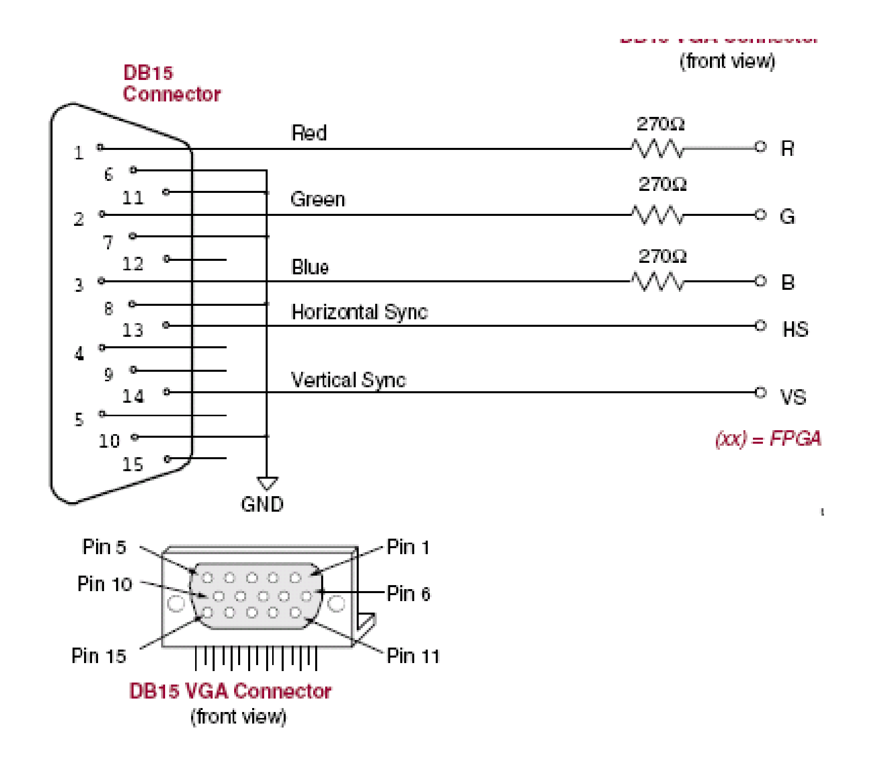



*Table 5-2:* **3-Bit Display Color Codes**

| Red (R) | Green (G) | Blue (B) | Resulting Color |
|---|---|---|---|
| 0 | 0 | 0 | Black |
| 0 | 0 | 1 | Blue |
| 0 | 1 | 0 | Green |
| 0 | 1 | 1 | Cyan |
| 1 | 0 | 0 | Red |
| 1 | 0 | 1 | Magenta |
| 1 | 1 | 0 | Yellow |
| 1 | 1 | 1 | White |

```
Net "IO_VGA_VSYNC"   LOC = "P168" ;   ##A1_IO41
Net "IO_VGA_HSYNC"   LOC = "P167" ;   ##A1_IO42
Net "IO_VGA_B"        LOC = "P172" ;   ##A1_IO43
Net "IO_VGA_G"        LOC = "P171" ;   ##A1_IO44
Net "IO_VGA_R"        LOC = "P178" ;   ##A1_IO45
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P168 | A1_IO41 | IO_VGA_VSYNC | VSYNC | U8_PIN14 |
| P167 | A1_IO42 | IO_VGA_HSYNC | HSYNC | U8_PIN13 |
| P172 | A1_IO43 | IO_VGA_B | BLUE | U8_PIN3 |
| P171 | A1_IO44 | IO_VGA_G | GREEN | U8_PIN2 |
| P178 | A1_IO45 | IO_VGA_R | RED | U8_PIN1 |



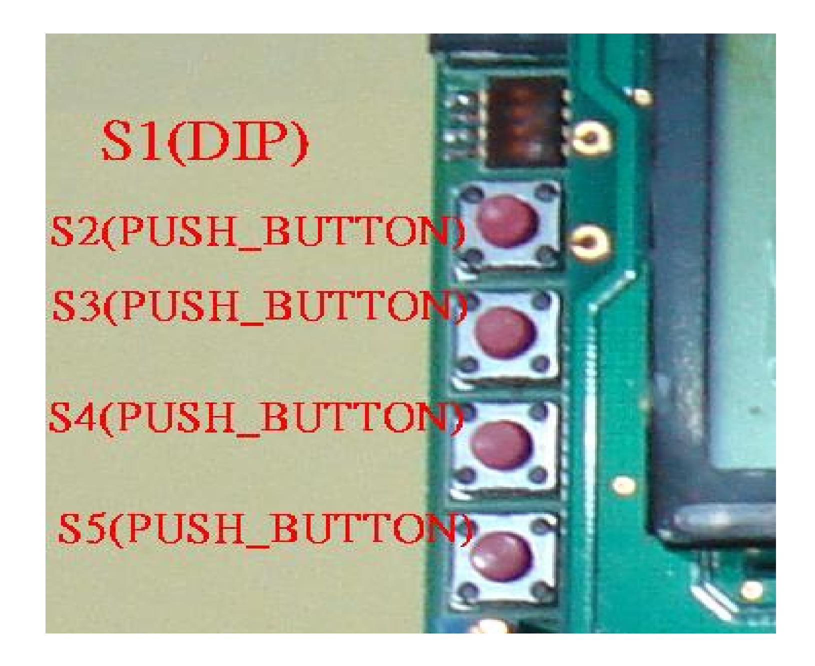
# 3-10. PUSH BUTTON

HUMAN_IO 提供四個按鍵與四個 DIP_SWICTH,位於板子的最左方,當 PUSH_BUTTON 按下時,輸入的電壓準位爲低電位’0’;當不按時爲’1’
當 DIP_SWITCH 往下切爲[ON]時,輸入電壓準位爲低電位’0’;而上切時爲[OFF].

```
NET "IO_DIP_SWITCH<0>"   LOC = "P138"   ;
NET "IO_DIP_SWITCH<1>"   LOC = "P137"   ;
NET "IO_DIP_SWITCH<2>"   LOC = "P140"   ;
NET "IO_DIP_SWITCH<3>"   LOC = "P139"   ;

NET "IO_PUSH_BUTTON<0>"   LOC = "P133"   ;
NET "IO_PUSH_BUTTON<1>"   LOC = "P132"   ;
NET "IO_PUSH_BUTTON<2>"   LOC = "P135"   ;
NET "IO_PUSH_BUTTON<3>"   LOC = "P134"   ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P138 | IO_DIP1 | USER_SW1 | 切爲 ON 時,輸入爲’0’ | IO_S1_1 |
| P137 | IO_DIP2 | USER_SW2 | 切爲 ON 時,輸入爲’0’ | IO_S1_2 |
| P140 | IO_DIP3 | USER_SW3 | 切爲 ON 時,輸入爲’0’ | IO_S1_3 |
| P139 | IO_DIP4 | USER_SW5 | 切爲 ON 時,輸入爲’0’ | IO_S2_4 |
| P133 | IO_SW1 | USER_DIP1 | 按下時,輸入爲’0’ | IO_S5 |
| P132 | IO_SW2 | USER_DIP2 | 按下時,輸入爲’0’ | IO_S4 |
| P135 | IO_SW3 | USER_DIP3 | 按下時,輸入爲’0’ | IO_S3 |
| P134 | IO_SW4 | USER_DIP4 | 按下時,輸入爲’0’ | IO_S2 |



# 3-11. ROTARY

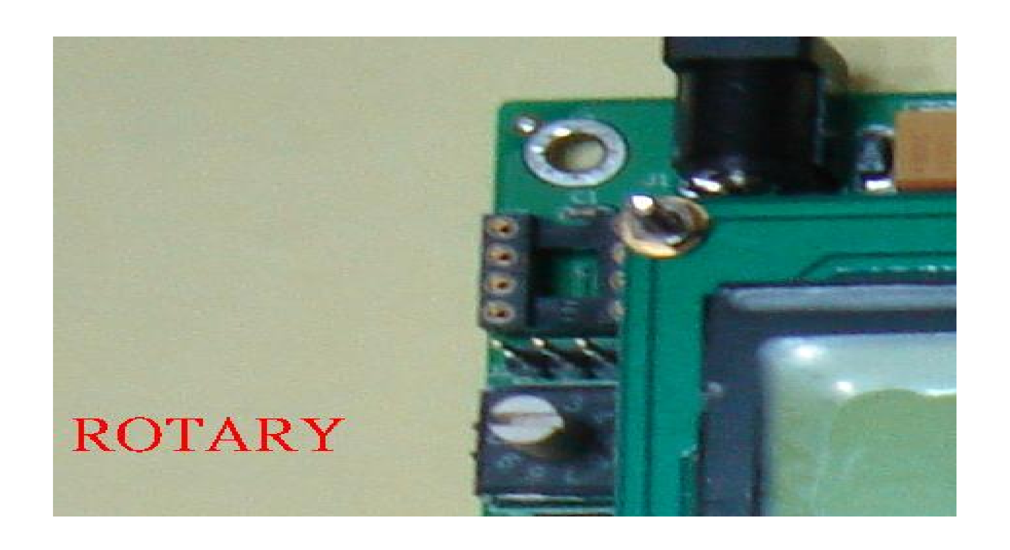
HUMAN_IO 提供一個按鍵與 ROTARY SWICTH,位於板子的最左方

```
NET "IO_ROTARY<0>"   LOC = "P145"   ;
NET "IO_ROTARY<1>"   LOC = "P147"   ;
NET "IO_ROTARY<2>"   LOC = "P144"   ;
NET "IO_ROTARY<3>"   LOC = "P146"   ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P145 | IO_ROTARY<0> | A2_IO41 | | |
| P147 | IO_ROTARY<1> | A2_IO42 | | |
| P144 | IO_ROTARY<2> | A2_IO43 | | IO_S3 |
| P146 | IO_ROTARY<3> | A2_IO44 | | IO_S2 |

當 ROTARY 切換到位置 0~9 時,IO_ROTARY<0> ~ IO_ROTARY<3>會輸出相對應的值,其值列表如下

| POSITION | IO_ROTARY<3> | IO_ROTARY<2> | IO_ROTARY<1> | IO_ROTARY<1> |
|---|---|---|---|---|
| **0** | 1 | 1 | 1 | 1 |
| **1** | 1 | 1 | 1 | 0 |
| **2** | 1 | 1 | 0 | 1 |
| **3** | 1 | 1 | 0 | 0 |
| **4** | 1 | 0 | 1 | 1 |
| **5** | 1 | 0 | 1 | 0 |
| **6** | 1 | 0 | 0 | 1 |
| **7** | 1 | 0 | 0 | 0 |
| **8** | 0 | 1 | 1 | 1 |
| **9** | 0 | 1 | 1 | 0 |

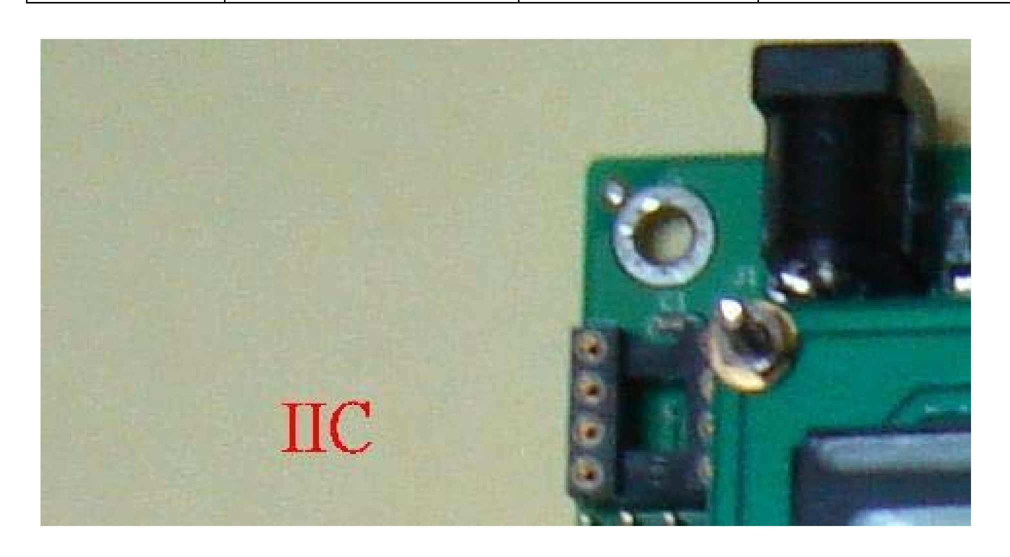


## 3-12. IIC

HUMAN_IO 提供 IIC 的 FLASH,編號為 24C02

```
NET "IO_IIC_SCL"    LOC = "P151"    ;
NET "IO_IIC_SDA"    LOC = "P150"    ;
```

| FPGA PIN | SYMBOL | LABEL NAME | LOGIC | COMMENT |
|---|---|---|---|---|
| P151 | IO_IIC_SCL | A2_IO45 | | U7_PIN6 |
| P150 | IO_IIC_SDA | A2_IO46 | | U7_PIN5 |

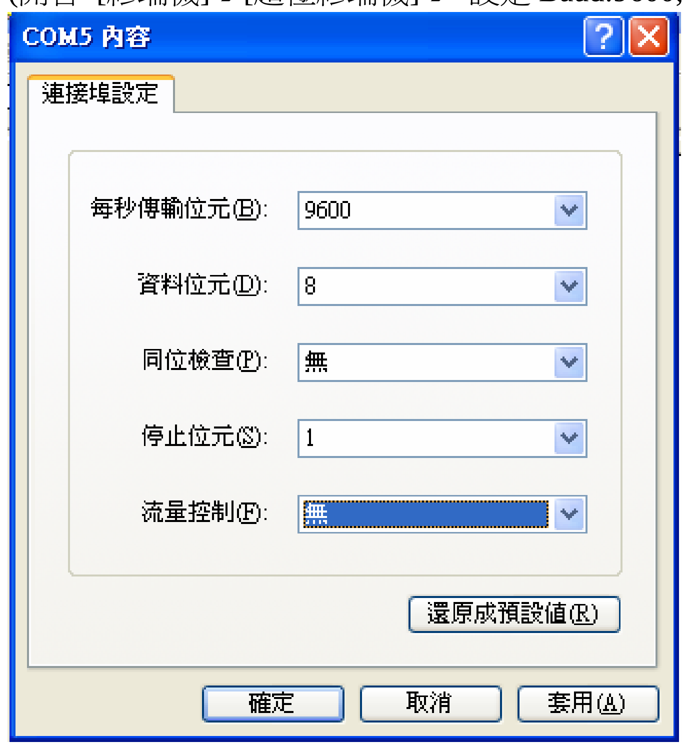


# 第四章 ：Ulinx_MB_XC3S250E_PQ208 測試

**4-1.**先安裝 **ISE** 軟體,序號由 **CD** 片中取得.

**4-2.**連接系統,建立測試環境.

4-2-1. 連接 DB25 的 1 對 1 測試線到 PC_Printer_Port 與 XC3S250E 板子的 P1(JTAG)
4-2-2. 連接電源(DC+5V/3A) 到 ULINX_MB_XC3S250E 板. ➔ J8 中間爲+5V
4-2-3. 連接 RS232 測試頭,以 1 對 1 的 DB9 延長線連接到個人電腦的 COM Port (開啓 [終端機]➔[超極終端機]➔ 設定 Baud:9600,Data:8,Stop:1,No Parity.)



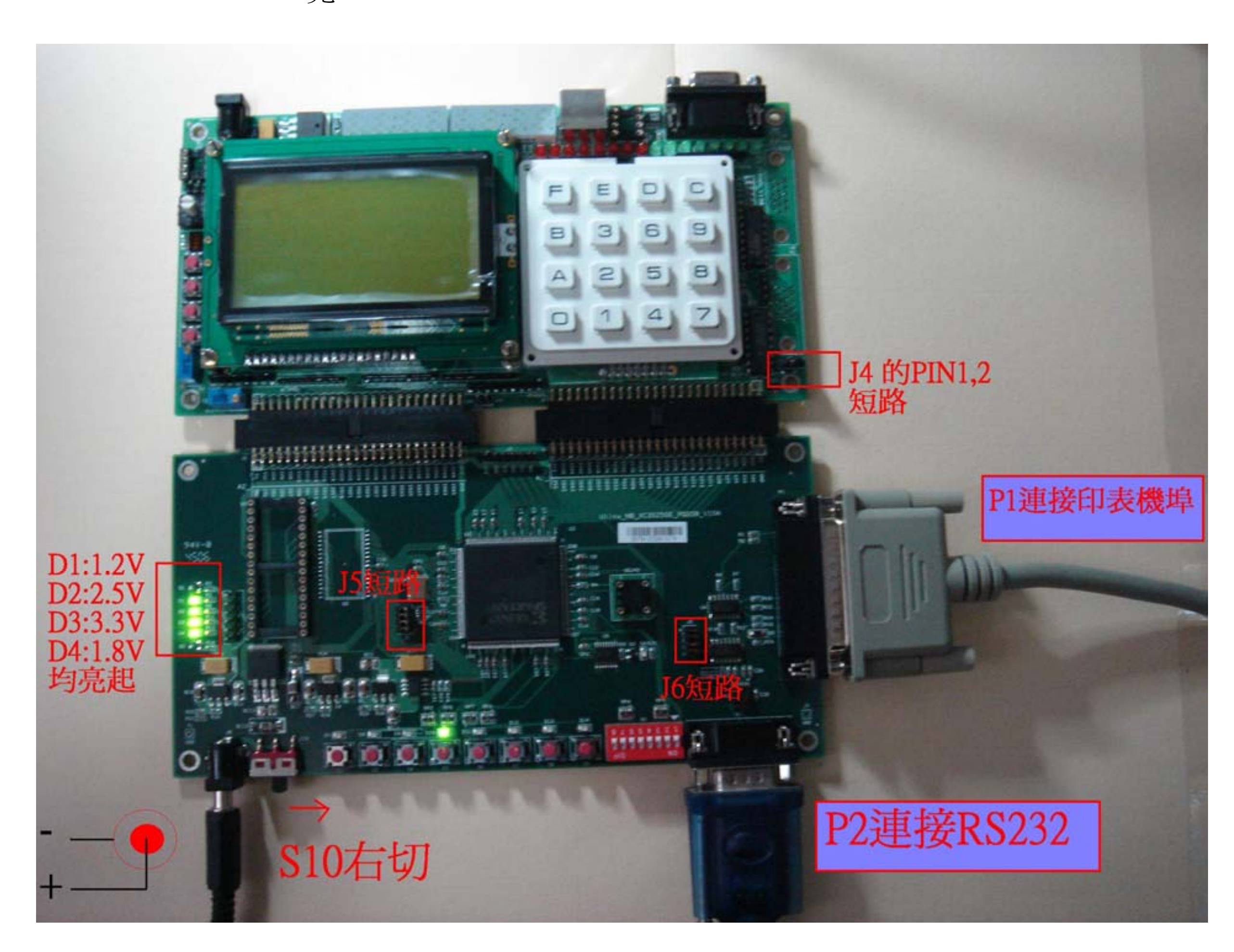

4-2-4. 設定板子的設定.

**J6 :** 短路(**4** 個短路 **pin)**
**J5 :** 短路(**4** 個短路 **pin)**
**J4 : 1,2** 短路(左邊兩隻腳短路).
其餘 **open**

4-2-5. R8,R9 先調整於 VR 的中間;確認連線

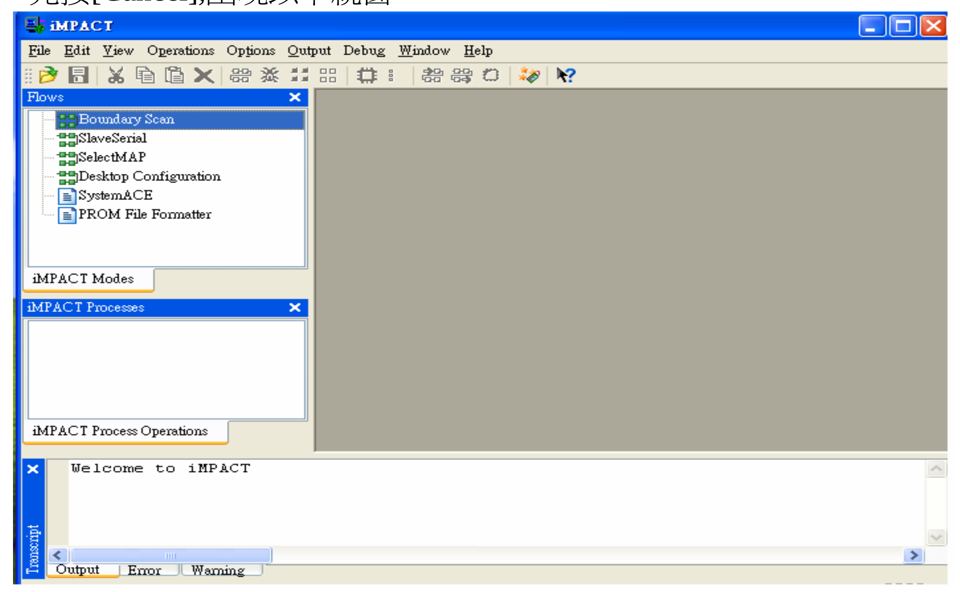
4-2-6. 將 S10 扳向右邊位置,開啓 DC+5V/3A 的電源,檢查電源的 LED 燈是否正常.

D1/1.2V： 亮
D2/2.5V： 亮
D3/3.3V： 亮
D4/1.8V： 亮

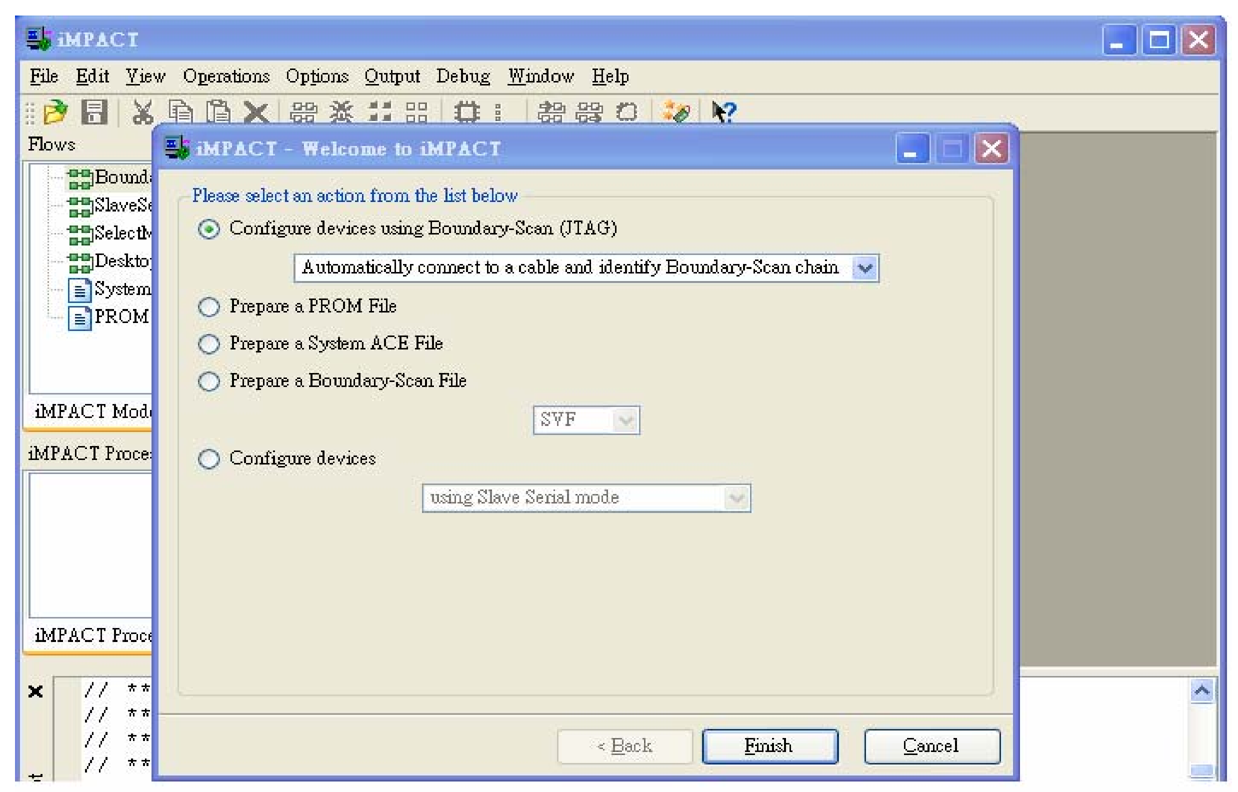


**4-3.開啓 Impact 的軟體**

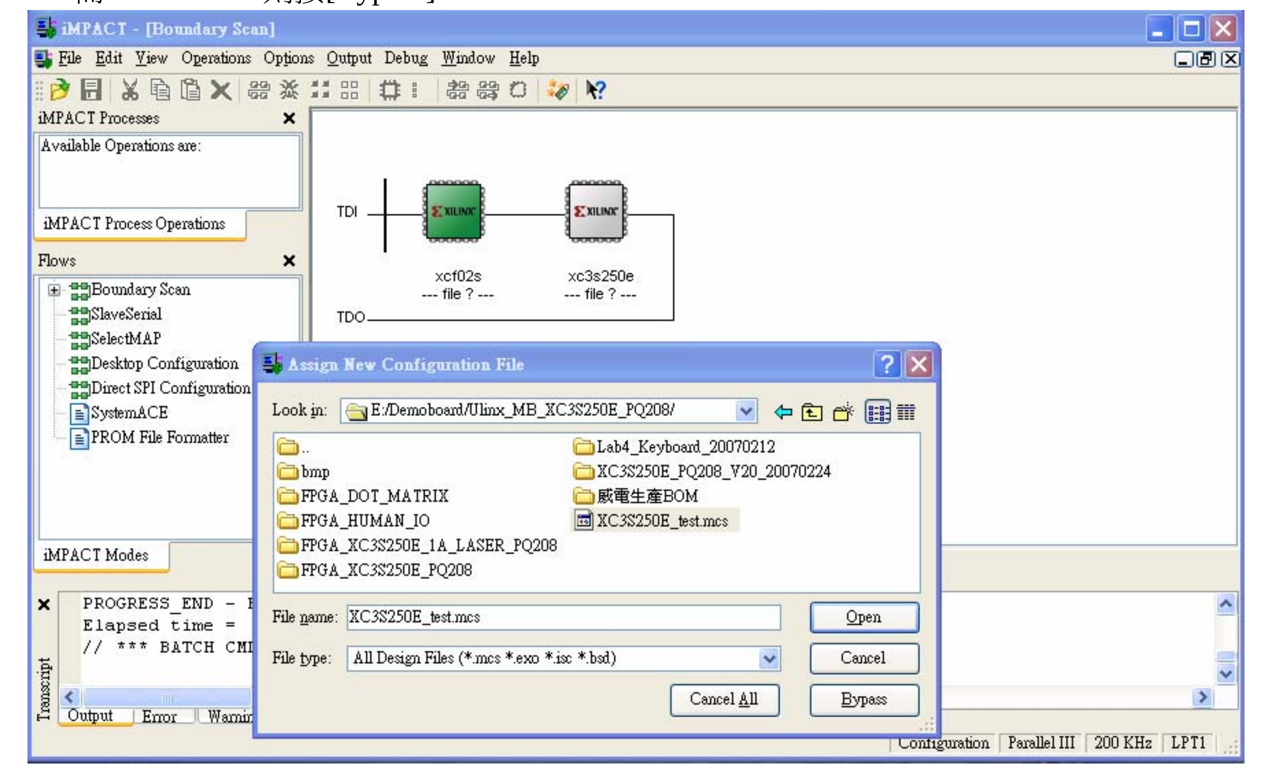
4-3-1. [開始]➔[程式集]➔[Xilinx ISE 8.1i]➔[Accessories] ➔ [Impact]
先按[Cancel],出現以下視窗。



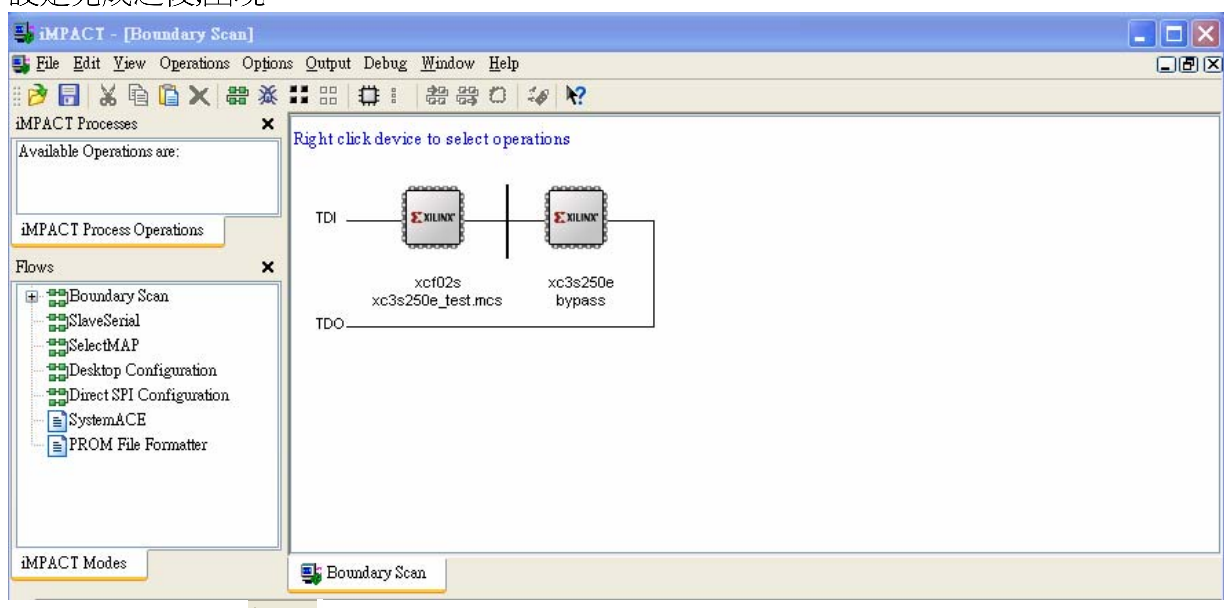

4-3-2. [File]➔[New] ➔ [Cancel]
[Edit]➔[Launch Wizard…] ➔ 選擇[Configure Device using Boundary-Scan(JTAG)]
➔ 按[Finish]




4-3-3.此時 JTAG 會自動偵測到 XCF02 與 XC3S400 兩顆元件,並顯示於螢幕上,
而同時指定 XCF08 的燒錄檔案為 XC3S250E_test.mcs
而 XC3S250E 則按[Bypass].

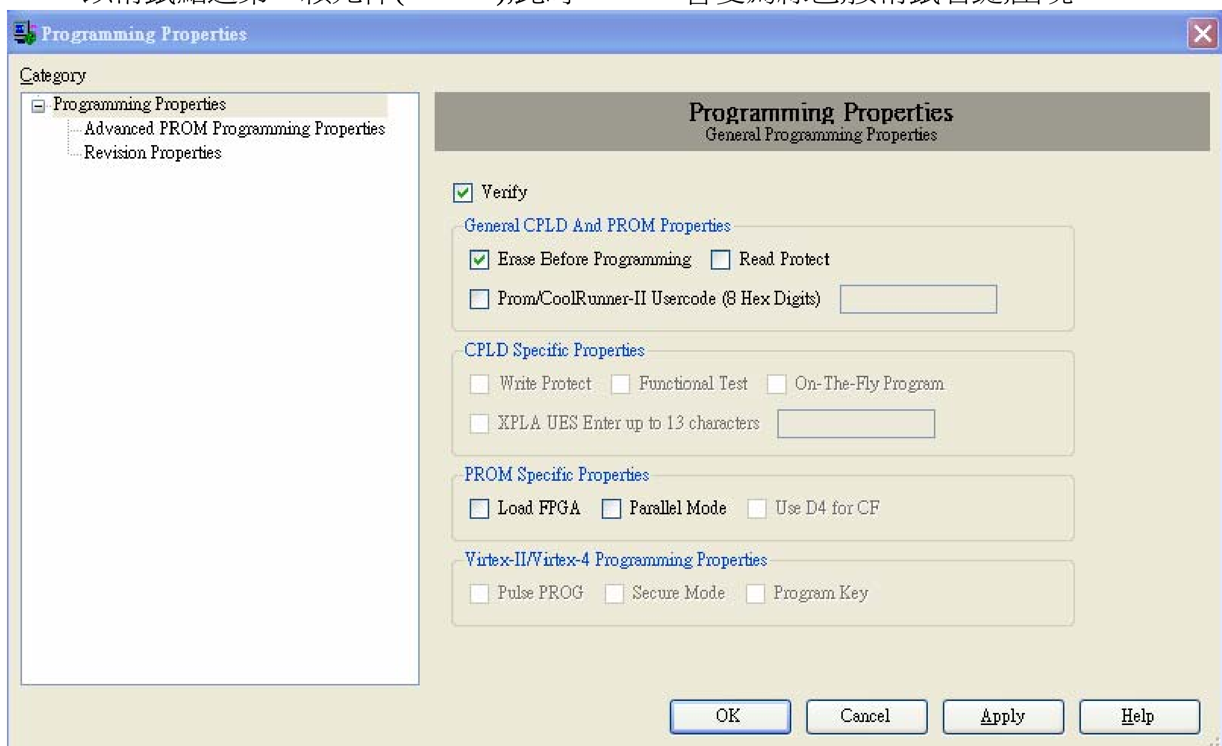


設定完成之後,出現




[Note]: 亦可以以[ ]開啓以上的畫面.

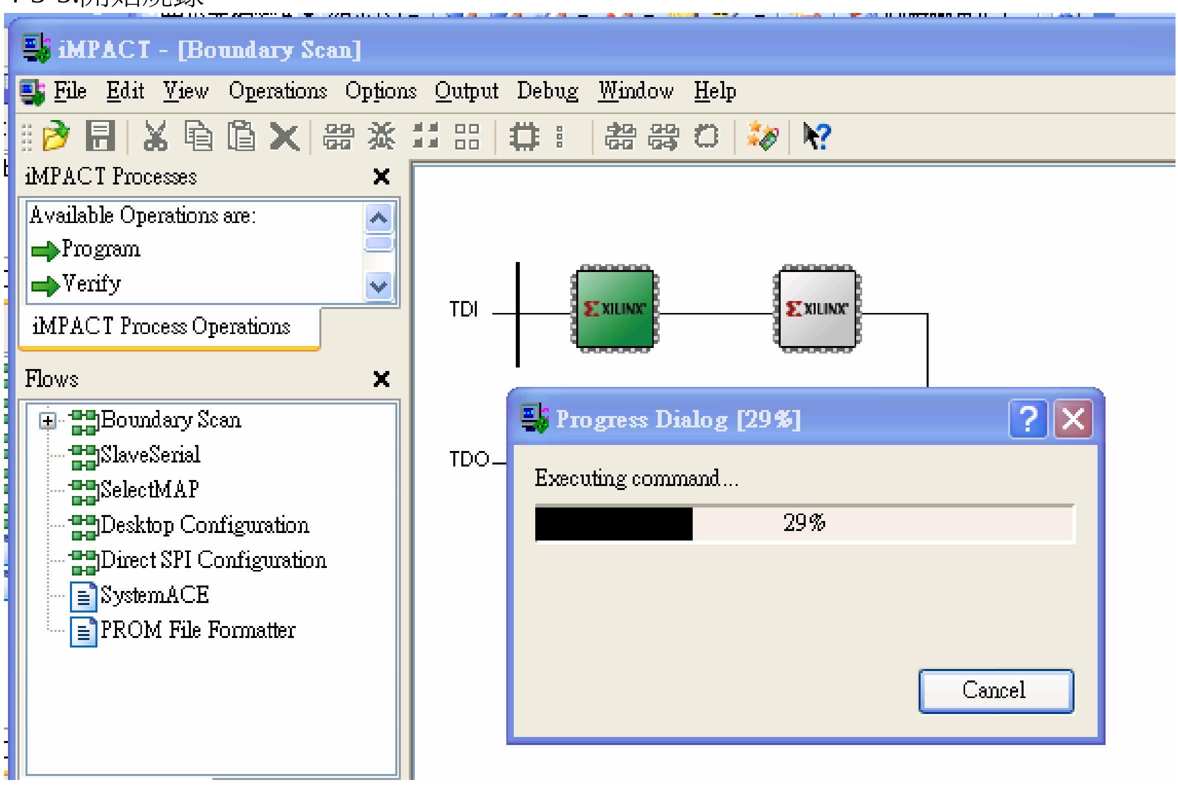
4-3-4.以滑鼠點選第一顆元件(XCF02),此時 XCF02 會變爲綠色,按滑鼠右鍵,出現



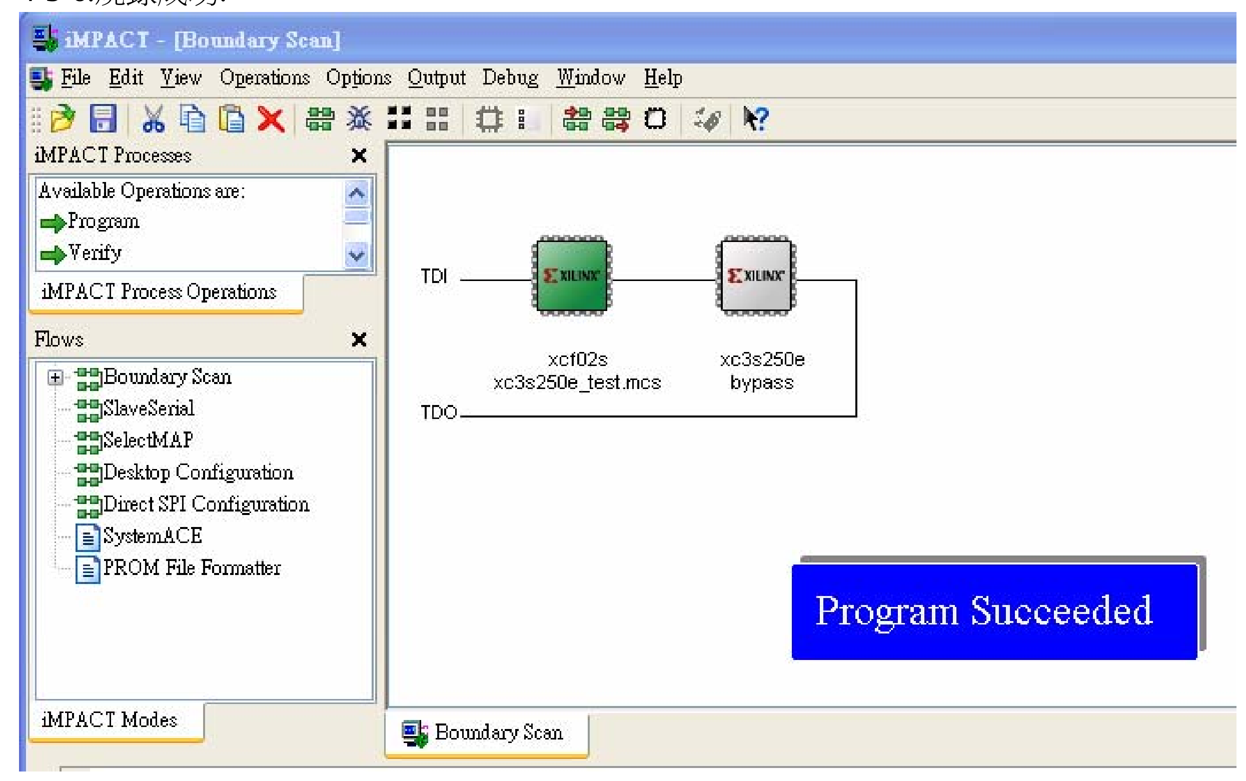

[Verify] 與 [Erase Before Programming] 需打勾 ➔ 然後按[OK]

***[Note]: 若是第一次燒錄, [Erase Before Programming] 可以不需打勾

4-3-5.開始燒錄




4-3-6.燒錄成功.



**4-4.開始驗證.**

4-4-1 關機後,重新開啓電源.D6/Done 亮起

4-4-2. 旋轉 R10(向左) ,調整 LCD 螢幕的亮度到適當.LCD 會出現
(可以旋轉 R9 向右, 使背景亮度變亮).

**爲希科技 Rot=0**
**KeyBoard = ?**
**SW=11111111 1111**
**DP =11111111 1111**

4-4-3. 按 FPGA 板的[S2],[S3],[S4],[S5],[S6],[S7],[S8],[S9] ➔ LCD 的 SW 前 8 位元相對位元會變爲 0

4-4-4. 按 HUMAN_IO 板的[S1],[S2],[S3],[S4] ➔ LCD 的 SW 後 4 位元相對位元會變爲 0

4-4-5. 切換 FPGA 板的 S1
將 S1-1 切到[ON] ,則 LCD 相對應的 DP : 11111110 1111
將 S1-2 切到[ON] ,則 LCD 相對應的 DP : 11111101 1111
將 S1-3 切到[ON] ,則 LCD 相對應的 DP : 11111011 1111
將 S1-4 切到[ON] ,則 LCD 相對應的 DP : 11110111 1111
將 S1-5 切到[ON] ,則 LCD 相對應的 DP : 11101111 1111
將 S1-6 切到[ON] ,則 LCD 相對應的 DP : 11011111 1111
將 S1-7 切到[ON] ,則 LCD 相對應的 DP : 10111111 1111
將 S1-8 切到[ON] ,則 LCD 相對應的 DP : 01111111 1111

4-4-6. 切換 HUMAN_IO 板的 S1
將 S1-1 切到[ON] ,則 LCD 相對應的 DP : 11111111 1110
將 S1-2 切到[ON] ,則 LCD 相對應的 DP : 11111111 1101
將 S1-3 切到[ON] ,則 LCD 相對應的 DP : 11111111 1011
將 S1-4 切到[ON] ,則 LCD 相對應的 DP : 11111111 0111

4-4-7. 按 KEY4X4 的按鍵.

按住[F]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = F
按住[E]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = E
按住[D]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = D
按住[C]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = C
按住[B]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = B
按住[3]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 3
按住[6]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 6
按住[9]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 9
按住[A]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = A
按住[2]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 2
按住[5]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 5
按住[8]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 8
按住[0]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 0
按住[1]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 1
按住[4]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 4
按住[7]鍵 ➔ LCD 的 KeyBoard 會出現 KeyBoard = 7

4-4-8. 七節燈管,出現

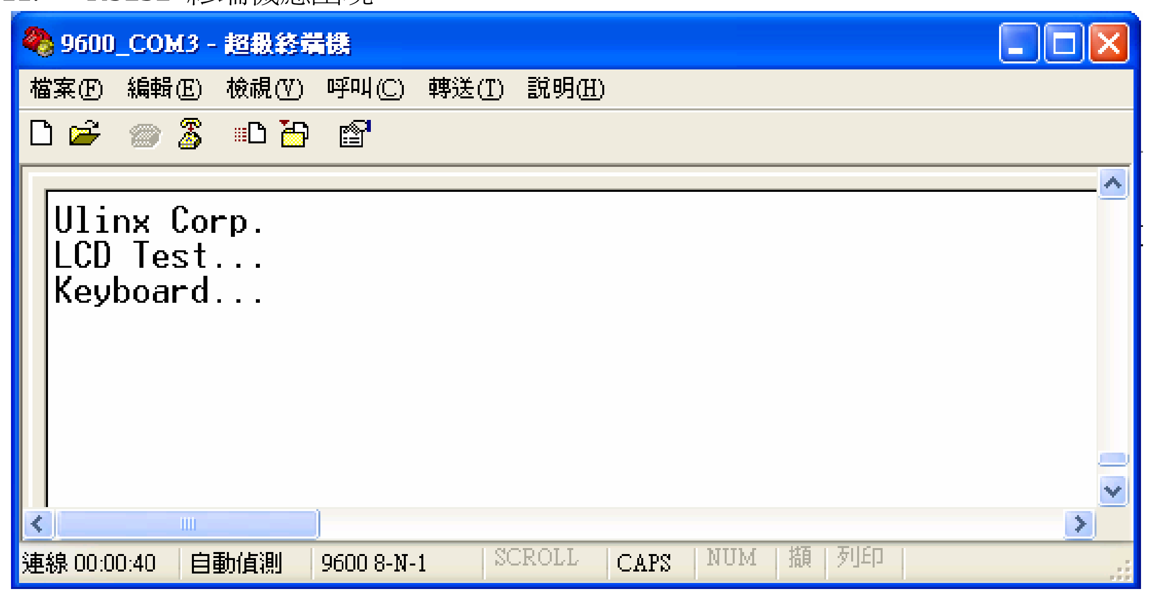
00000000 => 00010001 => 00020002 => 00030003 ……..一直往上計數

4-4-9. 旋轉 HUMAN_IO 的 ROTARY.

位置 0 ➔ LCD 的 Rot 會出現 Rot = 0
位置 1 ➔ LCD 的 Rot 會出現 Rot = 1
位置 2 ➔ LCD 的 Rot 會出現 Rot = 2
位置 3 ➔ LCD 的 Rot 會出現 Rot = 3
位置 4 ➔ LCD 的 Rot 會出現 Rot = 4
位置 5 ➔ LCD 的 Rot 會出現 Rot = 5
位置 6 ➔ LCD 的 Rot 會出現 Rot = 6
位置 7 ➔ LCD 的 Rot 會出現 Rot = 7
位置 8 ➔ LCD 的 Rot 會出現 Rot = 8
位置 9 ➔ LCD 的 Rot 會出現 Rot = 9

4-4-10. FPGA 板與 HUMAN_IO 板的 LED 共有 24 個 LED,會以右移方式,一直持續的顯示.

4-4-11.　RS232 終端機應出現




4-4-12. Finished!

